

# TH71101

315/433MHz

FSK/ASK Receiver

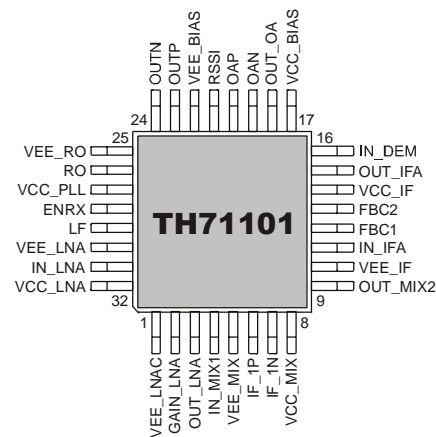
## Features

- Single-conversion superhet architecture for low external component count
- FSK demodulation with phase-coincidence demodulator
- Low current consumption in active mode and very low standby current
- Switchable LNA gain for improved dynamic range
- RSSI allows signal strength indication and ASK detection
- 32-pin Low profile Quad Flat Package (LQFP)

## Application Examples

- General digital data transmission
- Tire Pressure Monitoring Systems (TPMS)
- Remote Keyless Entry (RKE)
- Wireless access control
- Alarm and security systems
- Garage door openers
- Remote Controls
- Home and building automation
- Low-power telemetry systems

## Pin Description



## Ordering information

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
TH71101	E	NE	CAA-000	RE
TH71101	E	NE	CAA-000	TR

### Legend:

Temperature Code: E for Temperature Range -40°C to 85°C  
Package Code: NE for LQFP  
Packing Form: RE for Reel, TR for Tray  
Ordering example: TH71101ENE-CAA-000-RE

## General Description

The TH71101 FSK/ASK single-conversion superheterodyne receiver IC is designed for applications in the European 433MHz industrial-scientific-medical (ISM) band, according to the EN 300 220 telecommunications standard. It can also be used for any other system with carrier frequencies ranging from 300MHz to 450MHz (e.g. for applications according to FCC part 15 and ARIB STD-T67).

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## 1. Theory of Operation

### 1.1. General

With the TH71101 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FSK reception the IF tank used in the phase coincidence demodulator can be constituted by an external ceramic discriminator. In ASK configuration, the RSSI signal is fed to an ASK detector, which is constituted by the operational amplifier.

A double-conversion variant, called TH71102, is also available. This receiver IC allows a higher degree of image rejection, achieved in conjunction with an RF front-end filter. Both RXICs have the same die. At the TH71102, the second mixer (MIX2) is used to down-convert the first IF (IF1) to the second IF (IF2). At the TH71101, MIX2 operates as an amplifier.

Efficient RF front-end filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding an LC filter at the LNA output.

The TH71101 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) for generation of the local oscillator signal LO, parts of the PLL SYNTH are: the high-frequency VCO1, the feedback divider DIV\_16, a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the IF
- IF pre amplifier which is a mixer cell (MIX2) that operates as an amplifier
- IF amplifier (IFA) to amplify and limit the IF signal and for RSSI generation
- Phase coincidence demodulator (DEMOD) with third mixer (MIX3) to demodulate the IF signal
- Operational amplifier (OA) for data slicing, filtering and ASK detection
- Bias circuitry for bandgap biasing and circuit shutdown

### 1.2. Technical Data Overview

- |  |   |
|--|---|
| ▪ Input frequency range: 300 to 450 MHz  | ▪ Range of IF: 400 kHz to 22 MHz  |
| ▪ Power supply range: 2.3 to 5.5 V @ ASK | ▪ Maximum input level: -10 dBm @ ASK  |
| ▪ Temperature range: -40 to +85 °C       | ▪ 0 dBm @ FSK   |
| ▪ Standby current: 50 nA                 | ▪ Image rejection: > 45 dB (e.g. with 433.92 MHz SAW front-end filter and at 10.7 MHz IF) |
| ▪ Operating current: 6.5 mA @ low gain   | ▪ Spurious emission: < -70 dBm  |
| ▪ 8.2 mA @ high gain                     | ▪ Input frequency acceptance range: up to ±100 kHz  |
| ▪ Sensitivity: -113 dBm @ ASK 1)         | ▪ RSSI range: 70 dB   |
| ▪ -107 dBm @ FSK 2)                      | ▪ FSK deviation range: ±2.5 kHz to ±80 kHz  |
| ▪ Maximum data rate: 260 kbps NRZ @ ASK  |   |
| ▪ 180 kbps NRZ @ FSK                     |   |

1) at 4 kbps NRZ, BER =  $3 \cdot 10^{-3}$ , 180 kHz IF filter BW, without SAW front-end-filter loss

2) at 4 kbps NRZ, BER =  $3 \cdot 10^{-3}$ , ± 20 kHz FSK deviation, 180 kHz IF filter BW, without SAW front-end-filter loss

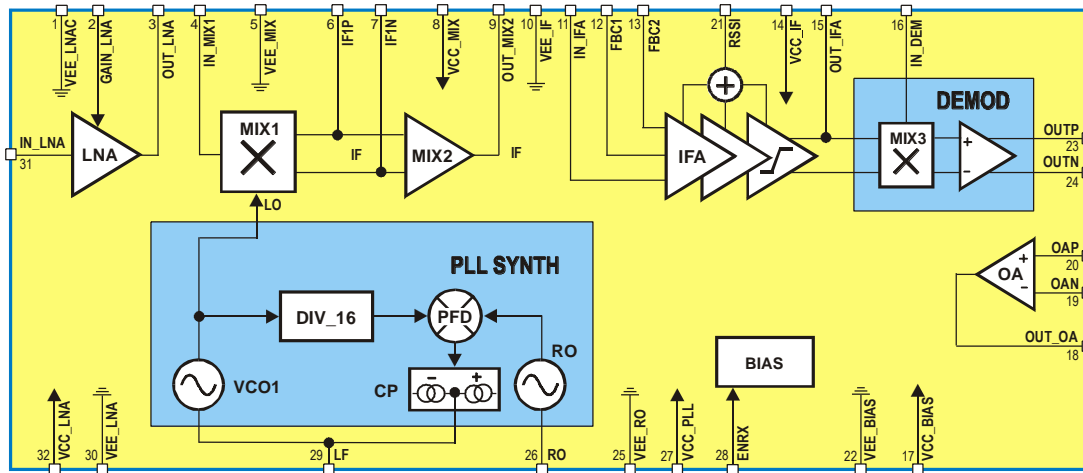


Fig. 1: TH71101 block diagram

### 1.4. Mode Configurations

ENRX	Mode	Description
0	RX standby	RX disabled
1	RX active	RX enable

*Note: ENRX are pulled down internally*

### 1.5. LNA GAIN Control

V <sub>GAIN_LNA</sub>	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain
> 1.4 V	LOW GAIN	LNA set to low gain

*Note: hysteresis between gain modes to ensure stability*

### 1.6. Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that can be chosen, and then the only possible choice is low-side or high-side injection of the LO signal (which is now the one and only LO signal in the receiver).

The receiver's single-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them is the image of the RF signal that must be suppressed by the RF front-end filter.

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By using the internal PLL synthesizer of the TH71101 with the fixed feedback divider ratio of  $N = 16$  (DIV\_16), two types of down-conversion are possible: low-side injection of LO and high-side injection of LO. The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF) and the LO frequency, for a given RF and IF.

Injection type	low	high
REF	$(RF - IF)/16$	$(RF + IF)/16$
LO	$16 \bullet REF$	$16 \bullet REF$
IF	$RF - LO$	$LO - RF$
RF image	$RF - 2IF$	$RF + 2IF$

### 1.6.1. Selected Frequency Plans

The following table depicts crystal, LO and image signals considering the examples of 315 MHz and 433.92 MHz RF reception at IF = 10.7 MHz.

Signal type	RF = 315 MHz	RF = 315 MHz	RF = 433.92 MHz	RF = 433.92 MHz
Injection type	low	<b>high</b>	<b>low</b>	high
REF / MHz	19.01875	<b>20.35625</b>	<b>26.45125</b>	27.78875
LO / MHz	304.3	<b>325.7</b>	<b>423.22</b>	444.62
RF image / MHz	293.6	<b>336.4</b>	<b>412.52</b>	455.32

The selection of the reference crystal frequency is based on some assumptions. As for example: the image frequency should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO signal should be in the range of 300 MHz to 450 MHz (because this is the optimum frequency range of the VCO1). Furthermore the IF should be as high as possible to achieve highest RF image rejection. The columns in bold depict the selected frequency plans to receive at 315 MHz and 433.92 MHz, respectively.

### 1.6.2. Maximum Frequency Coverage

Parameter	$f_{\min}$	$f_{\max}$
Injection type	high	low
RF / MHz	289.3	460.7
REF / MHz	18.75	28.125
LO / MHz	300	450
IF / MHz	10.7	10.7

## 2. Pin Definitions and Descriptions

Pin No.	Name	I/O Type	Functional Schematic	Description
3	OUT_LNA	analog output		LNA open-collector output, to be connected to external LC tank that resonates at RF
31	IN_LNA	analog input		LNA input, approx. 26Ω single-ended
1	VEE_LNAC	ground		ground of LNA core (cascode)
2	GAIN_LNA	analog input		LNA gain control (input with hysteresis)  RX standby: no pull-up RX active: pull-up
4	IN_MIX1	analog input		MIX1 input, approx. 33Ω single-ended
5	VEE_MIX	ground		ground of MIX1 and MIX2
6	IF1P	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
7	IF1N	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
8	VCC_MIX	supply		positive supply of MIX1 and MIX2
9	OUT_MIX2	analog output		MIX2 output, approx. 330Ω output impedance
10	VEE_IF	ground		ground of IFA and DEMOD

Pin No.	Name	I/O Type	Functional Schematic	Description
11	IN_IFA	analog input		IFA input, approx. 2.2kΩ input impedance
12	FBC1	analog I/O		to be connected to external IFA feedback capacitor
13	FBC2	analog I/O		to be connected to external IFA feedback capacitor
14	VCC_IF	supply		positive supply of IFA and DEMOD
15	OUT_IFA	analog I/O		IFA output and MIX3 input (of DEMOD)
16	IN_DEM	analog input		DEMOM input, to MIX3 core
17	VCC_BIAS	supply		positive supply of general bias system and OA
18	OUT_OA	analog output		OA output, 40uA current drive capability
19	OAN	analog input		negative OA input
20	OAP	analog input		positive OA input

Pin No.	Name	I/O Type	Functional Schematic	Description
21	RSSI	analog output		RSSI output, for RSSI and ASK detection, approx. 36kΩ output impedance
22	VEE_BIAS	ground		ground of general bias system and OA
23	OUTP	analog output		FSK positive output, output impedance of 100kΩ to 300kΩ
24	OUTN	analog output		FSK negative output, output impedance of 100kΩ to 300kΩ
25	VEE_RO	ground		ground of DIV, PFD, RO and charge pump
26	RO	analog input		RO input, Colpitts type oscillator with internal feedback capacitors
27	VCC_PLL	supply		positive supply of DIV, PFD, RO and charge pump
28	ENRX	digital input		mode control input, CMOS-compatible with internal pull-down circuit
29	LF	analog I/O		charge pump output and VCO1 control input
30	VEE_LNA	ground		ground of LNA biasing
32	VCC_LNA	supply		positive supply of LNA biasing



### 3. Technical Data

#### 3.1. Absolute Maximum Ratings

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	$V_{CC}$		0	7.0	V
Input voltage	$V_{IN}$		-0.3	$V_{CC}+0.3$	V
Input RF level	$P_{iRF}$	@ LNA input		10	dBm
Storage temperature	$T_{STG}$		-40	+125	°C
Junction temperature	$T_J$			+150	°C
Thermal Resistance	$R_{thJA}$			60	K/W
Power dissipation	$P_{diss}$			0.1	W
Electrostatic discharge	$V_{ESD1}$	human body model, 3)	-1.0	+1.0	kV
	$V_{ESD2}$	human body model, 4)	-0.75	+0.75	

3) all pins except OUT\_LNA, IF1P and IF1N

4) pin OUT\_LNA, IF1P and IF1N

#### 3.2. Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	$V_{CC,FSK}$	0 °C to 85 °C	2.5	5.5	V
		-20 °C to 85 °C	2.6	5.5	
		-40 °C to 85 °C	2.7	5.5	
	$V_{CC,ASK}$	-40 °C to 85 °C	2.3	5.5	
Operating temperature	$T_A$		-40	+85	°C
Input low voltage (CMOS)	$V_{IL}$	ENRX pin		$0.3 \cdot V_{CC}$	V
Input high voltage (CMOS)	$V_{IH}$	ENRX pin	$0.7 \cdot V_{CC}$		V
Input frequency range	$f_i$		289.3	460.7	MHz
IF range	$f_{IF}$		0.4	22	MHz
XOSC frequency	$f_{ref}$	set by the crystal	18.75	28.125	MHz
VCO frequency	$f_{LO}$	$f_{LO} = 16 \cdot f_{ref}$	300	450	MHz
Frequency deviation	$\Delta f$		$\pm 2.5$	$\pm 80$	kHz
FSK data rate	$R_{FSK}$	NRZ, C15 = NIP, 5)		180	kbps
ASK data rate	$R_{ASK}$	NRZ, C16 = NIP, 5)		260	kbps

5)  $B_{IF} = 400$  kHz,  $P_{IN} = -90$  dBm

#### 3.3. Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	$f_0$	fundamental mode, AT	18.75	28.125	MHz
Load capacitance	$C_L$		10	15	pF
Static capacitance	$C_0$			7	pF
Series resistance	$R_1$			50	$\Omega$

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**3.4. DC Characteristics**

all parameters under normal operating conditions, unless otherwise stated;  
 typical values at  $T_A = 23\text{ }^\circ\text{C}$  and  $V_{CC} = 3\text{ V}$

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Operating Currents</b>						
Standby current	$I_{SBY}$	ENRX=0		50	100	nA
Supply current at low gain	$I_{CC, low}$	ENRX=1 GAIN_LNA=1	4.0	6.5	12.0	mA
Supply current at high gain	$I_{CC, high}$	ENRX=1 GAIN_LNA=0	4.5	8.2	14.0	mA
<b>Digital Pin Characteristics</b>						
Input low voltage CMOS	$V_{IL}$	ENRX pin	-0.3		$0.3 \cdot V_{CC}$	V
Input high voltage CMOS	$V_{IH}$	ENRX pin	$0.7 \cdot V_{CC}$		$V_{CC} + 0.3$	V
Pull down current ENRX pin	$I_{PDEN}$	ENRX=1	0.1	2	10	$\mu\text{A}$
Low level input current ENRX pin	$I_{INLEN}$	ENRX=0			0.05	$\mu\text{A}$
<b>Analog Pin Characteristics</b>						
High level input current GAIN_LNA pin	$I_{INHAIN}$	GAIN_LNA=1			0.05	$\mu\text{A}$
Pull up current GAIN_LNA pin active	$I_{PUGAINa}$	GAIN_LNA=0 ENRX=1	0.08	0.15	0.3	$\mu\text{A}$
Pull up current GAIN_LNA pin standby	$I_{PUGAINs}$	GAIN_LNA=0 ENRX=0			0.05	$\mu\text{A}$
High gain input voltage	$V_{IHAIN}$	ENRX=1			0.7	V
Low gain input voltage	$V_{ILGAIN}$	ENRX=1	1.5			V
<b>Opamp Characteristics</b>						
Opamp input offset voltage	$V_{offs}$		-35		35	mV
Opamp input offset current	$I_{offs}$	$I_{OAP} - I_{OAN}$	-50		50	nA
Opamp input bias current	$I_{bias}$	$0.5 \cdot (I_{OAP} + I_{OAN})$	-150		150	nA
<b>RSSI Characteristics</b>						
RSSI voltage at low input level	$V_{RSSI, low}$	$P_i = -65\text{ dBm}$ , GAIN_LNA=1	0.5	1.0	1.5	V
RSSI voltage at high input level	$V_{RSSI, high}$	$P_i = -35\text{ dBm}$ , GAIN_LNA=1	1.2	1.9	2.5	V

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**3.5. AC System Characteristics**

all parameters under normal operating conditions, unless otherwise stated;

typical values at  $T_A = 23\text{ }^\circ\text{C}$  and  $V_{CC} = 3\text{ V}$ ,

RF at 433.92 MHz; SAW frond-end filter loss and IF at 10.7 MHz;

all parameters based on test circuits as shown in Fig. 2, Fig.3 and Fig. 5

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Receive Characteristics</b>						
Input sensitivity – FSK (standard)	$P_{\min, ST}$	$B_F = 180\text{kHz}$ , $\Delta f = \pm 20\text{kHz}$ , 4kbps NRZ, $BER \leq 3 \cdot 10^{-3}$ , 6)		-104		dBm
Input sensitivity – FSK (narrow band)	$P_{\min, NB}$	$B_F = 30\text{kHz}$ , $\Delta f = \pm 5\text{kHz}$ , 4kbps NRZ, $BER \leq 3 \cdot 10^{-3}$ , 6)		-108		dBm
Input sensitivity – ASK	$P_{\min, ASK}$	$B_F = 180\text{kHz}$ , 4kbps NRZ, $BER \leq 3 \cdot 10^{-3}$ , 6)		-110		dBm
Maximum input signal – FSK	$P_{\max, FSK}$	$BER \leq 3 \cdot 10^{-3}$ GAIN_LNA = 1		0		dBm
Maximum input signal – ASK	$P_{\max, ASK}$	$BER \leq 3 \cdot 10^{-3}$ GAIN_LNA = 1		-10		dBm
Spurious emission	$P_{\text{spur}}$				-70	dBm
Image rejection	$\Delta P_{\text{imag}}$			45		dB
<b>Start-up Parameters</b>						
Crystal start-up time	$T_{\text{XTL}}$	ENRX from 0 to 1			0.9	ms
Receiver start-up time	$T_{\text{RX}}$	ENRX from 0 to 1, depends on data slicer time constant, valid data at output			$T_{\text{XTL}}$ + $R4 \cdot C17$	
<b>PLL Parameters</b>						
VCO gain	$K_{\text{VCO}}$			250		MHz/V
Charge pump current	$I_{\text{CP}}$			60		$\mu\text{A}$

6) incl. 3 dB loss of front-end SAW filter

## 4. Test Circuits

### 4.1. Standard FSK Reception

#### 4.1.1. Standard FSK Application Circuit

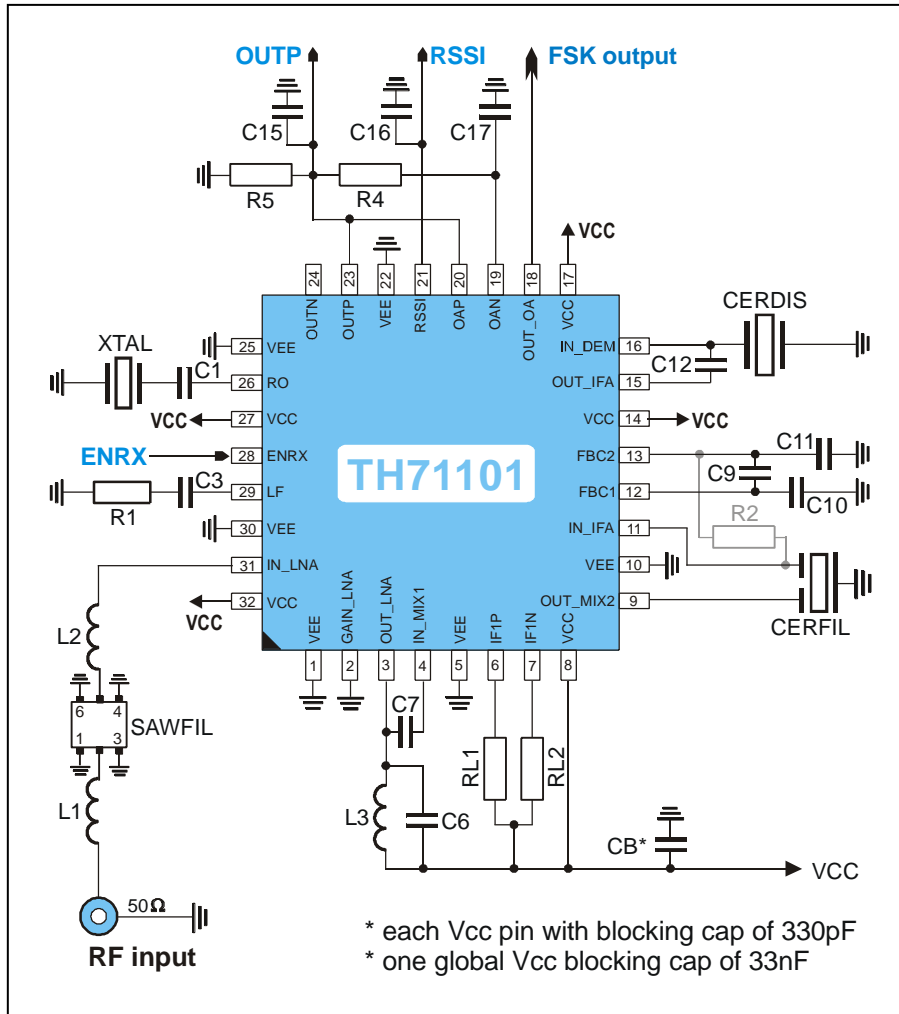


Fig. 2: Test circuit for FSK reception

#### Circuit Features

- Tolerates input frequency variations
- Well-suited for NRZ, Manchester and similar codes

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**4.1.2. Standard FSK Component List**

Part	Size	Value @ 433.92 MHz	Tolerance	Description
C1	0805	27 pF	±5%	crystal series capacitor
C3	0603	1 nF	±10%	loop filter capacitor
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C9	0603	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0805	10 pF	±5%	DEMODO phase-shift capacitor
C15	0805	100 pF	±5%	demodulator output low-pass capacitor, this value for data rates < 20 kbps NRZ
C16	0805	1.5 nF	±10%	RSSI output low-pass capacitor
C17	0805	10 nF	±10%	data slicer capacitor, this value for data rates > 0.8 kbps NRZ
R1	0603	10 kΩ	±5%	loop filter resistor
R2	0603	330 Ω	±5%	optional CERFIL output matching resistor
R4	0805	330 kΩ	±5%	data slicer resistor
R5	0805	220 kΩ	±5%	loading resistor
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	68 nH	±5%	SAW filter matching inductor from Würth-Elektronik (WE-KI series), or equivalent part
L2	0603	82 nH	±5%	
L3	0603	15 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
XTAL	SMD 6x3.5	26.45125 MHz @ RF = 433.92 MHz	±25ppm cal. ±30ppm temp.	fundamental-mode crystal from Telcona/Horizon or equivalent part
SAWFIL	SMD 3x3	SAFCC433MBLOX00 (f <sub>0</sub> = 433.92 MHz)	B <sub>3dB</sub> = 840 kHz	low-loss SAW filter from Murata, or equivalent part
CERFIL	SMD 3.45x3.1	SFECF10M7HA00	B <sub>3dB</sub> = 180 kHz	ceramic filter from Murata, or equivalent part
CERDIS	SMD 4.5x2	CDSCB10M7GA135		ceramic discriminator from Murata, or equivalent part

- For component values for other frequencies, please refer to the EVB descriptions



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**4.2.2. Narrow Band FSK Component List**

Part	Size	Value @ 433.92 MHz	Tolerance	Description
C1	0805	27 pF	±5%	crystal series capacitor
C3	0603	1 nF	±10%	loop filter capacitor
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C9	0603	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0805	1.5 pF	±5%	DEMODO phase-shift capacitor
C15	0805	220 pF	±5%	demodulator output low-pass capacitor, this value for data rates < 10 kbps NRZ
C16	0805	1.5 nF	±10%	RSSI output low-pass capacitor
C17	0805	10 nF	±10%	data slicer capacitor, this value for data rates > 0.8 kbps NRZ
CP	0603	6.8 - 8.2 pF	±5%	ceramic resonator loading capacitor
R1	0603	10 kΩ	±5%	loop filter resistor
R2	0603	330 Ω	±5%	optional CERFIL output matching resistor
R4	0805	330 kΩ	±5%	data slicer resistor
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	68 nH	±5%	SAW filter matching inductor from Würth-Elektronik (WE-KI series), or equivalent part
L2	0603	82 nH	±5%	
L3	0603	15 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
XTAL	SMD 6x3.5	26.45125 MHz @ RF = 433.92 MHz	±25ppm cal. ±30ppm temp.	fundamental-mode crystal from Telcona/Horizon or equivalent part
SAWFIL	SMD 3x3	SAFCC433MBLOX00 (f <sub>0</sub> = 433.92 MHz)	B <sub>3dB</sub> = 840 kHz	low-loss SAW filter from Murata, or equivalent part
CERFIL	Leaded type	SFKLA10M7NL00	B <sub>3dB</sub> = 30 kHz	ceramic filter from Murata, or equivalent part
		SFVLA10M7LF00	B <sub>3dB</sub> = 80 kHz	optional, ceramic filter from Murata, or equivalent part
CERDIS	SMD 4.5x2	CDSCB10M7GA135		ceramic discriminator from Murata, or equivalent part

- For component values for other frequencies, please refer to the EVB descriptions

### 4.3. ASK Reception

#### 4.3.1. ASK Application Circuit

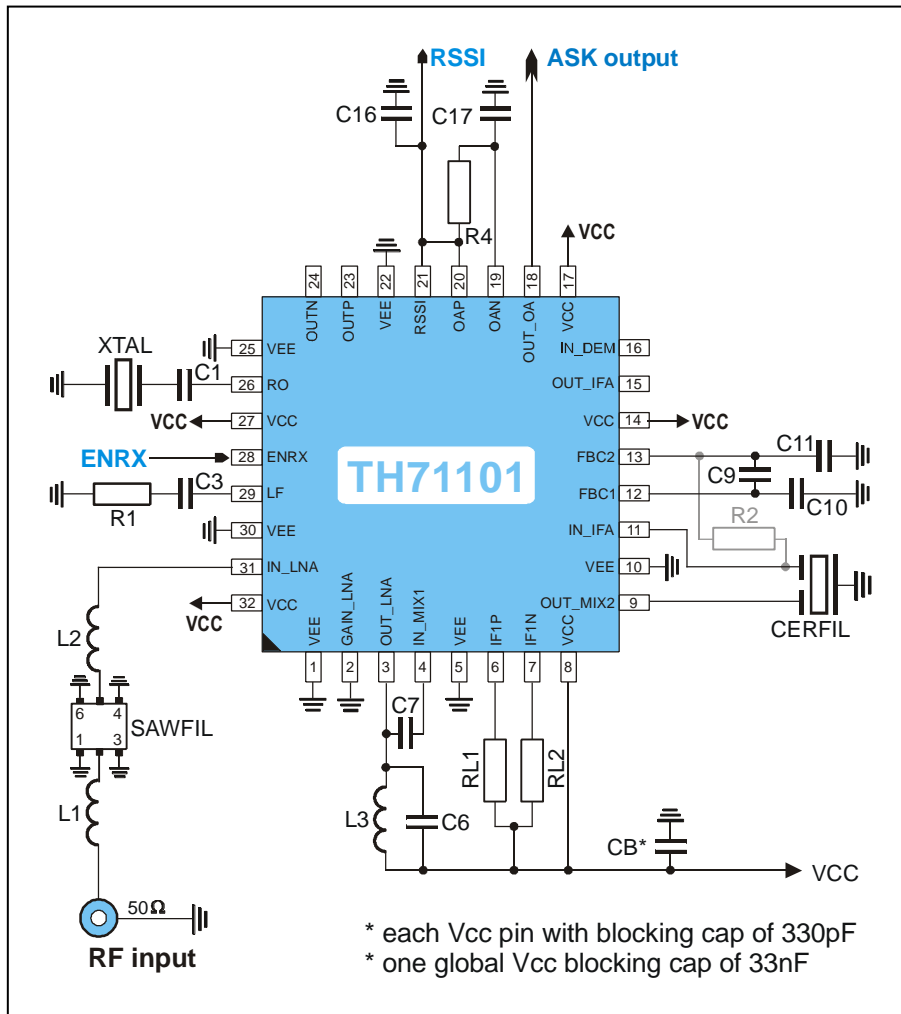


Fig. 5: Test circuit for ASK reception



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**4.3.2. ASK Component List**

Part	Size	Value @ 433.92 MHz	Tolerance	Description
C1	0805	27 pF	±5%	crystal series capacitor
C3	0603	1 nF	±10%	loop filter capacitor
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C9	0603	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C16	0805	1.5 nF	±10%	RSSI output low-pass capacitor, this value for data rates < 10 kbps NRZ
C17	0805	10 nF	±10%	data slicer capacitor, this value for data rates > 0.8 kbps NRZ
R1	0603	10 kΩ	±5%	loop filter resistor
R2	0603	330 Ω	±5%	optional CERFIL output matching resistor
R4	0805	330 kΩ	±5%	data slicer resistor
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	68 nH	±5%	SAW filter matching inductor from Würth-Elektronik (WE-KI series), or equivalent part
L2	0603	82 nH	±5%	
L3	0603	15 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
XTAL	SMD 6x3.5	26.45125 MHz @ RF = 433.92 MHz	±25ppm cal. ±30ppm temp.	fundamental-mode crystal from Telcona/Horizon or equivalent part
SAWFIL	SMD 3x3	SAFCC433MBLOX00 (f <sub>0</sub> = 433.92 MHz)	B <sub>3dB</sub> = 840 kHz	low-loss SAW filter from Murata, or equivalent part
CERFIL	SMD 3.45x3.1	SFECF10M7HA00	B <sub>3dB</sub> = 180 kHz	ceramic filter from Murata, or equivalent part
	Leaded type	SFVLA10M7LF00	B <sub>3dB</sub> = 80 kHz	optional, ceramic filter from Murata, or equivalent part

- For component values for other frequencies, please refer to the EVB descriptions

## 5. Package Description

The device TH71101 is RoHS compliant.

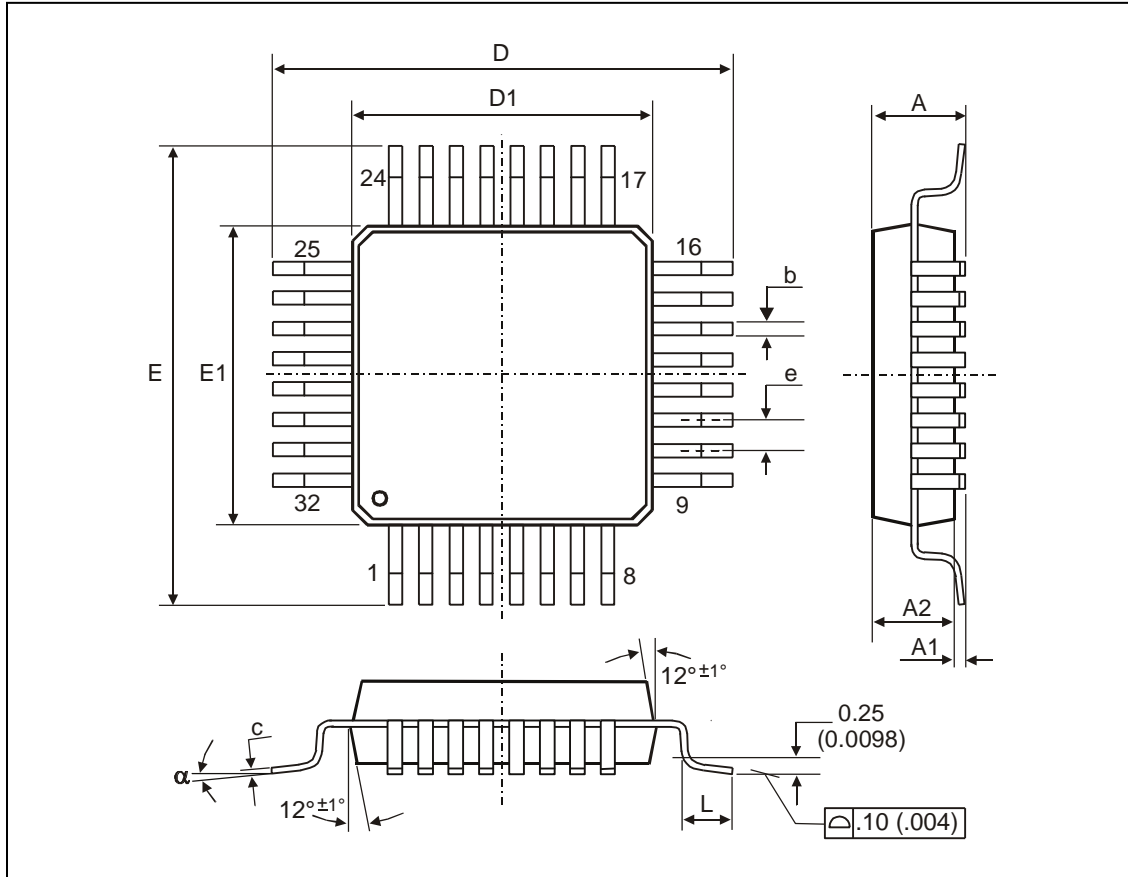


Fig. 6: LQFP32 (Low profile Quad Flat Package)

All Dimension in mm, coplanarity < 0.1mm										
	E1, D1	E, D	A	A1	A2	e	b	c	L	$\alpha$
min	7.00	9.00	1.40	0.05	1.35	0.8	0.30	0.09	0.45	0°
max			1.60	0.15	1.45		0.45	0.20		0.75
All Dimension in inch, coplanarity < 0.004"										
	E1, D1	E, D	A	A1	A2	e	b	c	L	$\alpha$
min	0.276	0.354	0.055	0.002	0.053	0.031	0.012	0.0035	0.018	0°
max			0.063	0.006	0.057		0.018	0.0079		0.030

### 5.1. Soldering Information

- The device TH71101 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20.

## 6. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

### Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020  
Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113  
Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

### Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20  
Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15  
Resistance to soldering temperature for through-hole mounted devices

### Iron Soldering THD's (Through Hole Devices)

- EN60749-15  
Resistance to soldering temperature for through-hole mounted devices

### Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21  
Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: <http://www.melexis.com/quality.aspx>

## 7. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

## 8. Contact

For the latest version of this document, go to our website at [www.melexis.com](http://www.melexis.com).

For additional information, please contact our Direct Sales team and get help for your specific needs:

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