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9DB106BFLFT

IDT

Clock Buffer 6 OUTPUT PCIE GEN2 BUFFER

Six Output Differential Buffer for PCIe Gen 2

9DB106

Description

The **9DB106** zero-delay buffer supports PCIe Gen1 and Gen2 clocking requirements. The **9DB106** is driven by a differential SRC output pair from an IDT CK410/CK505-compliant main clock generator. It attenuates jitter on the input clock and has a selectable PLL bandwidth to maximize performance in systems with or without Spread-Spectrum clocking. An SMBus interface allows control of the PLL bandwidth and bypass options, while 2 clock request (CLKREQ#) pins make the **9DB106** suitable for Express Card applications.

Recommended Applications

6 Output Differential Buffer for PCIe Gen 2

Output Features

- 6 - 0.7V current mode differential output pairs (HCSL)

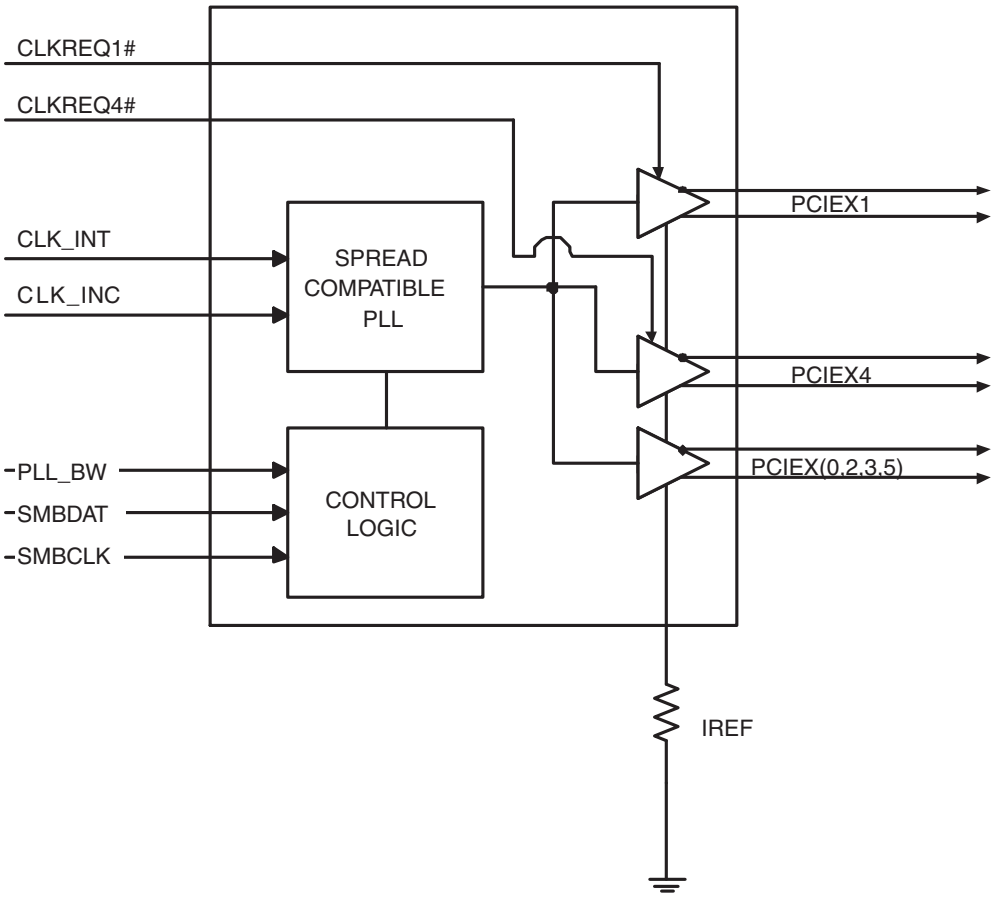
Features/Benefits

- CLKREQ# pin for outputs 1 and 4/ supports Express Card applications
- PLL or bypass mode/PLL can dejitter incoming clock
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- SMBus Interface/unused outputs can be disabled

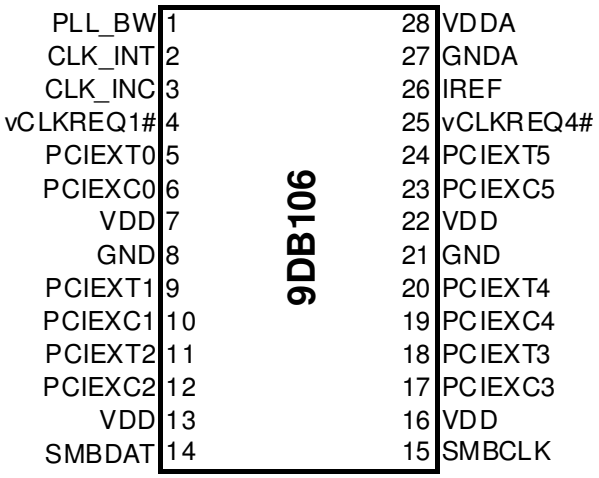
Key Specifications

- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50 ps

Functional Block Diagram



Pin Configuration



Note: Pins preceeded by ' v ' have internal 120K ohm pull down resistors

28-pin SSOP & TSSOP

Power Groups

Pin Number		Description
VDD	GND	
7, 13, 16, 22	8,21	PCI Express Outputs
TBD	TBD	SMBUS
N/A	27	IREF
28	27	Analog VDD & GND for PLL core

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	PLL_BW	IN	3.3V input for selecting PLL Band Width 0 = low, 1= high
2	CLK_INT	IN	True Input for differential reference clock.
3	CLK_INC	IN	Complementary Input for differential reference clock.
4	vCLKREQ1#	IN	Output enable for PCI Express output pair 1. 0 = enabled, 1 =disabled
5	PCIEXT0	OUT	True clock of differential PCI_Express pair.
6	PCIEXC0	OUT	Complementary clock of differential PCI_Express pair.
7	VDD	PWR	Power supply, nominal 3.3V
8	GND	IN	Ground pin.
9	PCIEXT1	OUT	True clock of differential PCI_Express pair.
10	PCIEXC1	OUT	Complementary clock of differential PCI_Express pair.
11	PCIEXT2	OUT	True clock of differential PCI_Express pair.
12	PCIEXC2	OUT	Complementary clock of differential PCI_Express pair.
13	VDD	PWR	Power supply, nominal 3.3V
14	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
15	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
16	VDD	PWR	Power supply, nominal 3.3V
17	PCIEXC3	OUT	Complementary clock of differential PCI_Express pair.
18	PCIEXT3	OUT	True clock of differential PCI_Express pair.
19	PCIEXC4	OUT	Complementary clock of differential PCI_Express pair.
20	PCIEXT4	OUT	True clock of differential PCI_Express pair.
21	GND	PWR	Ground pin.
22	VDD	PWR	Power supply, nominal 3.3V
23	PCIEXC5	OUT	Complementary clock of differential PCI_Express pair.
24	PCIEXT5	OUT	True clock of differential PCI_Express pair.
25	vCLKREQ4#	IN	Output enable for PCI Express output pair 4. 0 = enabled, 1 =disabled
26	IREF	OUT	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.
27	GNDA	PWR	Ground pin for the PLL core.
28	VDDA	PWR	3.3V power for the PLL core.

Note:
Pins preceeded by ' v ' have internal 120K ohm pull down resistors

Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	˚C	1
Junction Temperature	Tj				125	˚C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Input/Supply/Common Output Parameters

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	˚C	1
	T_{IND}	Industrial range	-40		85	˚C	1
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1,2
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1,2
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1,2
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1,2
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1,2
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;		130	150	mA	1
		all differential pairs tri-stated		30	40	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V	80	100	105	MHz	
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			4.5	pF	1
Clk Stabilization	T_{STAB}	From VDD reaching 3.1V and input clock stable			1.8	ms	1
Input Spread Spectrum Modulation Frequency		Triangular Modulation	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	cycles	1,3
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Except differential input clock

[3]Time from deassertion until outputs are >200mV

Electrical Characteristics - Clock Input Parameters

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics - PLL Parameters

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

Group	Parameter	Description	Min	Typ	Max	Units	Notes
PLL Jitter Peaking	$j_{peak-hibw}$	(PLL_BW = 1)	0	1	2.5	dB	1,4
PLL Jitter Peaking	$j_{peak-lobw}$	(PLL_BW = 0)	0	1	2	dB	1,4
PLL Bandwidth	pll_{HIBW}	(PLL_BW = 1)	2	2.5	3	MHz	1,5
PLL Bandwidth	pll_{LOBW}	(PLL_BW = 0)	0.4	0.5	1	MHz	1,5
Jitter, Phase	$t_{jphasePLL}$	PCIe Gen 1 phase jitter (1.5 - 22 MHz)		40	108	ps	1,2,3
		PCIe Gen 2 jitter (8-16 MHz, 5-16 MHz) Hi-Band >1.5MHz (PLL_BW=1)		2.7	3.1	ps rms	1,2,3
		PCIe Gen 2 jitter (8-16 MHz, 5-16 MHz) Hi-Band >1.5MHz (PLL_BW=0)		2.2	3.1	ps rms	1,2,3
		PCIe Gen 2 jitter (8-16 MHz, 5-16 MHz) Lo-Band <1.5MHz		1.3	3	ps rms	1,2,3

NOTES:

1. Guaranteed by design and characterization, not 100% tested in production.
2. See http://www.pcisig.com for complete specs
3. Device driven by 932S421BGLF or equivalent
4. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
5. Measured at 3 db down or half power point.

Electrical Characteristics - PCIEX 0.7V Current Mode Differential Outputs

TA = T_{COM} or T_{IND}; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			<	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1,3
Min Voltage	Vuds		-300				1,3
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1,3
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1,3
Long Accuracy	ppm	see Tperiod min-max values			0	ppm	1,2
Average period	T_{period}	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Input to Output Delay	t_{pd}	PLL Mode.	0		150	ps	1
	t_{pdbyp}	Bypass mode	3.7		4.2	ns	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Output-to-Output Skew	t_{sk3}	V_T = 50%		40	50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode, Measurement from differential wavefrom		35	50	ps	1
		BYPASS mode as additive jitter		35	50	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] The 9DB106 does not add a ppm error to the input clock.

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

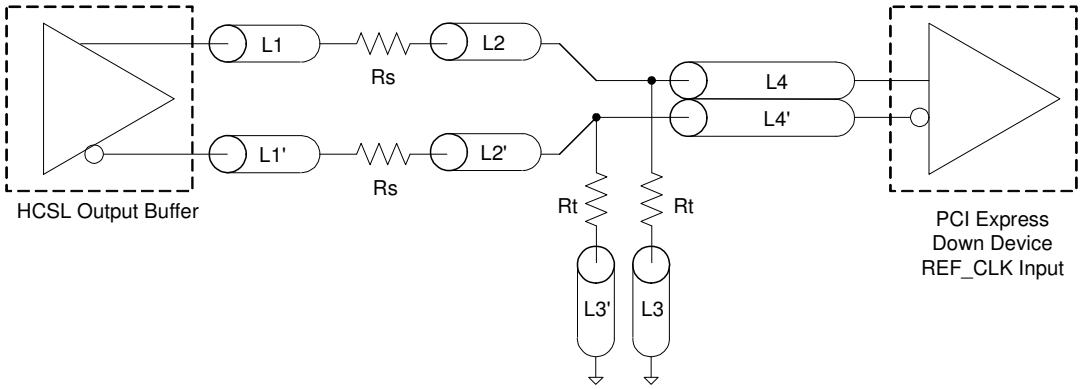
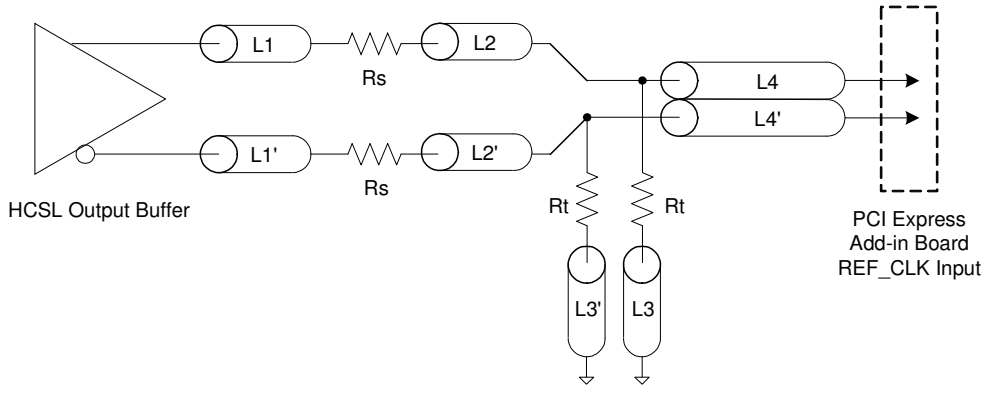


Figure 2: PCI Express Connector Routing

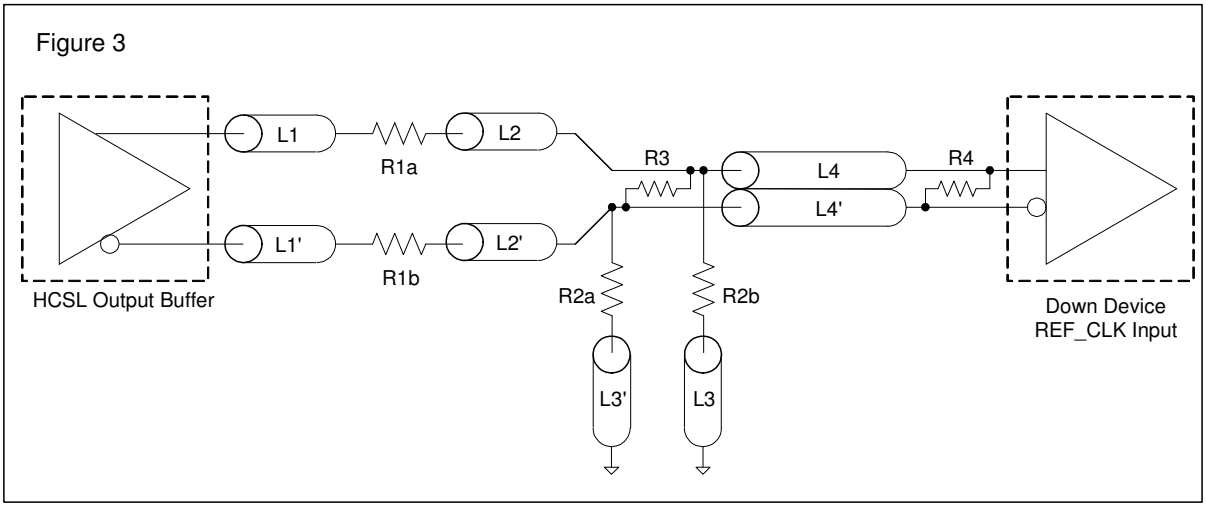


Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

R1a = R1b = R1

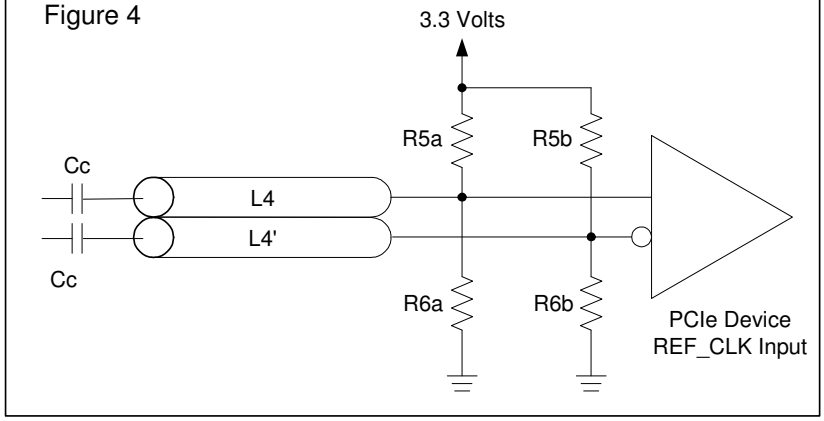
R2a = R2b = R2

Figure 3



Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



General SMBus serial interface information for the 9DB106

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D4_{(h)}$
- IDT clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- IDT clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- IDT clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***)
- IDT clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D4_{(h)}$
- IDT clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- IDT clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D5_{(h)}$
- IDT clock will ***acknowledge***
- IDT clock will send the data byte count = X
- IDT clock sends ***Byte N + X -1***
- IDT clock sends ***Byte 0 through byte X (if $X_{(h)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		IDT (Slave/Receiver)
T	starT bit	
Slave Address $D4_{(h)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
◇		
◇		◇
◇		◇
		◇
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		IDT (Slave/Receiver)	
T	starT bit		
Slave Address $D4_{(h)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D5_{(h)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			◇
◇			◇
◇			◇
◇			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBusTable: Device Control Register, READ/WRITE ADDRESS (D4/D5)

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SW_EN	Enables SMBus Control of bits (1:0)	RW	PLL controlled by SMBus registers	PLL controlled by device pins	1
Bit 6	-	RESERVED		RW	-		X
Bit 5	-	RESERVED		RW	-		X
Bit 4	-	RESERVED		RW	-		X
Bit 3	-	RESERVED		RW	-		X
Bit 2	-	RESERVED		RW	-		X
Bit 1	-	PLL BW #adjust	Selects PLL Bandwidth	RW	Low BW	High BW	1
Bit 0	-	PLL Enable	Bypasses PLL for board test	RW	PLL bypassed (fan out mode)	PLL enabled (ZDB mode)	1

SMBusTable: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RESERVED		RW	-		X
Bit 6	-	RESERVED		RW	-		X
Bit 5	24,23	PCIEX5	Output Control	RW	Disable	Enable	1
Bit 4	-	RESERVED		RW	-		X
Bit 3	18,17	PCIEX3	Output Control	RW	Disable	Enable	1
Bit 2	11,12	PCIEX2	Output Control	RW	Disable	Enable	1
Bit 1	-	RESERVED		RW	-		X
Bit 0	5,6	PCIEX0	Output Control	RW	Disable	Enable	1

SMBusTable: Function Select Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED		RW	-		X
Bit 6		RESERVED		RW	-		X
Bit 5	-	RESERVED		RW	-		X
Bit 4	-	RESERVED		RW	-		X
Bit 3	-	RESERVED		RW	-		X
Bit 2	-	RESERVED		RW	-		X
Bit 1	-	RESERVED		RW	-		X
Bit 0	-	RESERVED		RW	-		X

SMBusTable: Vendor & Revision ID Register

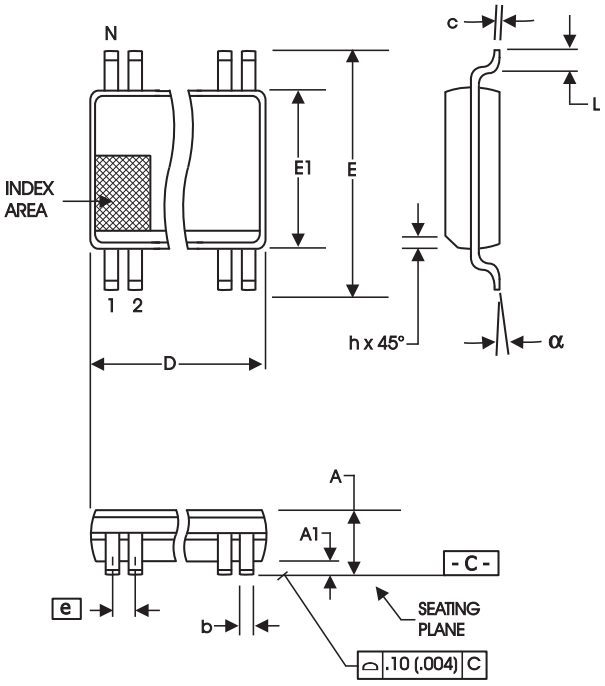
Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-			R	-		0
Bit 6	-			R	-		0
Bit 5	-			R	-		0
Bit 4	-		Device ID	R	-		0
Bit 3	-		= 06 Hex	R	-		0
Bit 2	-			R	-		1
Bit 1	-			R	-		1
Bit 0	-			R	-		0

SMBusTable: Byte Count Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7		RW	-	-	0
Bit 6	-	BC6	Writing to this	RW	-	-	0
Bit 5	-	BC5	register will	RW	-	-	0
Bit 4	-	BC4	configure how	RW	-	-	0
Bit 3	-	BC3	many bytes will be	RW	-	-	0
Bit 2	-	BC2	read back, default	RW	-	-	1
Bit 1	-	BC1	is 06 = 6 bytes.	RW	-	-	1
Bit 0	-	BC0		RW	-	-	0



209 mil SSOP

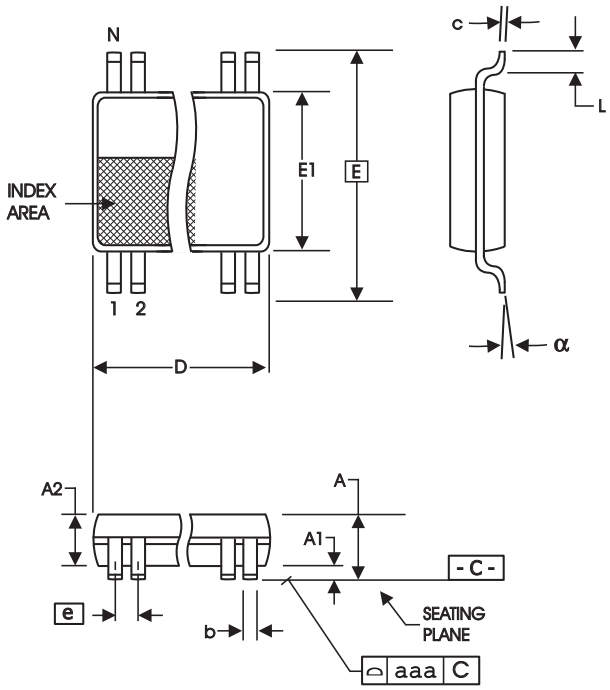
SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033



4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DB106BFLF	Tubes	28-pin SSOP	0 to +70°C
9DB106BFLFT	Tape and Reel	28-pin SSOP	0 to +70°C
9DB106BGLF	Tubes	28-pin TSSOP	0 to +70°C
9DB106BGLFT	Tape and Reel	28-pin TSSOP	0 to +70°C
9DB106BFILF	Tubes	28-pin SSOP	-40 to +85°C
9DB106BFILFT	Tape and Reel	28-pin SSOP	-40 to +85°C
9DB106BGILF	Tubes	28-pin TSSOP	-40 to +85°C
9DB106BGILFT	Tape and Reel	28-pin TSSOP	-40 to +85°C

"LF" after the package code are the Pb-Free configuration and are RoHS compliant.
"B" is the device revision designator (will not correlate to the datasheet revision).

Revision History

Rev.	Originator	Issue Date	Description	Page #
B	RDW	9/12/2005	1. Changed Output to Output skew from 30ps to 45ps. 2. Changed PLL mode jitter from 40ps to 35ps. 3. Changed Bypass mode additive jitter from 25ps to 35ps. 4. Updated LF Ordering Information.	5, 8-9
C	RDW	8/17/2006	Corrected Typo of SMBus Read/Write Address.	7
D	RDW	3/12/2007	Added SMBus Read/Write Table.	6
E	RDW	8/6/2007	1. Added Phase Noise Parameters, Updated input to output delay values. 2. PLL BW moved to PLL parameters table. 3. Added terminations tables.	6-8
F		12/14/2007	Updated SMBus serial Interface Information.	9
G	RDW	4/1/2010	Updated ordering info for Rev B	13
H	RDW	9/15/2010	1. Updated DS to include I-temp specs and ordering information 2. Updated electrical tables to reflect common set of numbers for I-temp and C-temp 3. Converted all references of ICS to IDT 4. Corrected placement of AC coupling caps in Figure 4	
J	RDW	1/27/2011	Updated Termination Figure 4.	8
K	RDW	4/20/2011	1. Changed pull down indicator from '**" to " v " to correct pin description of CLKREQ# pins.	
L	AT	5/24/2012	Added OE# Latency spec to Common Input/Output Parameters table	4

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