

### PWM INTELLIGENT POWER HIGH SIDE SWITCH

#### Features

- Integrated bootstrap for 100kHz switching
- Charge pump for DC operation
- Over temperature shutdown
- Over current shutdown
- 3.3V logic level
- Ground loss protection
- ESD protection

#### Applications

- 24V loads
- Injectors
- Valves
- DC motors

#### Description

The Device is a five terminal Intelligent Power Switch (IPS) for use in a high side configuration. It features short circuit, over-temperature, ESD protection, inductive load capability and diagnostic feedback. An integrated bootstrap diode allows fast switching.

#### Product Summary

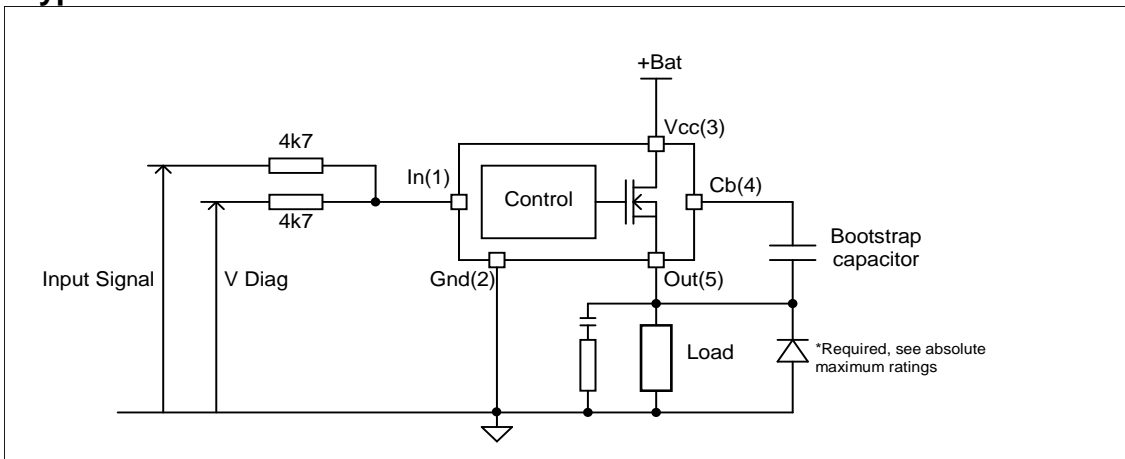
Rds(on)	35mΩ max.
Vbr	75V min.
I shutdown	25A(min.)

#### Package



D-Pak

#### Typical Connection



**Qualification Information†**

<b>Qualification Level</b>		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		DKAK-5L	MSL1, 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M2 (150V) (per AEC-Q100-003)	
	Human Body Model	Class H1A (500V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (1000V) (per AEC-Q100-011)	
<b>IC Latch-Up Test</b>		Class II, Level A (per AEC-Q100-004)	
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (T<sub>J</sub>= -40°C..150°C, V<sub>cc</sub>=6..60V unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
V <sub>out</sub>	Maximum output voltage	Gnd-3	V <sub>cc</sub> +0.3	V
V <sub>offset</sub>	Maximum logic ground to load ground offset	V <sub>cc</sub> -65	V <sub>cc</sub> +0.3	
V <sub>in</sub>	Maximum input voltage	-0.3	5.5	
V <sub>cc max.</sub>	Maximum V <sub>cc</sub> voltage	—	65	
I <sub>in max.</sub>	Maximum input current	-3	10	mA
P <sub>d</sub>	Maximum power dissipation (internally limited by thermal protection) R <sub>th</sub> =50°C/W 1"sq. footprint	—	2.5	W
T <sub>j max.</sub>	Max. storage & operating temperature junction temperature	-40	150	°C

## Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
R <sub>th1</sub>	Thermal resistance junction to ambient	50	—	°C/W
R <sub>th2</sub>	Thermal resistance junction to case	1.2	—	

## Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V <sub>IH</sub>	High level input voltage	2.7	5.5	V
V <sub>IL</sub>	Low level input voltage	0	0.9	
R <sub>in</sub>	Recommended resistor in series with IN pin	2(1)	10(2)	kΩ
R <sub>dg</sub>	Recommended resistor in series with dg pin	2(1)	10(2)	
F <sub>max.</sub>	Max. switching frequency	—	100	kHz
C <sub>boot</sub>	Bootstrap capacitor	30	50	nF

(1) limited by the maximum input current

(2) limited by the input capacitor

## Static Electrical Characteristics

T<sub>J</sub>=-40..150°C, V<sub>CC</sub>=6..60V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R <sub>ds(on)</sub>	ON state resistance T <sub>J</sub> =25°C	—	30	35	mΩ	V <sub>in</sub> =5V, I <sub>out</sub> =5A
	ON state resistance T <sub>J</sub> =150°C	—	50	70		V <sub>in</sub> =5V, I <sub>out</sub> =5A
V <sub>CC op.</sub>	Operating voltage range with short circuit protection	6	—	60	V	
I <sub>CC Off</sub>	Supply current during Sleep mode	—	0.2	5	μA	During sleep mode V <sub>in</sub> =0V, V <sub>out</sub> =0V T <sub>J</sub> =25°C, V <sub>CC</sub> =28V
I <sub>out Off</sub>	Output leakage current during Sleep mode	—	0.2	5		
I <sub>CC On</sub>	Supply current when On	—	4	10	mA	V <sub>in</sub> =5V T <sub>J</sub> =25°C, V <sub>CC</sub> =28V
I <sub>out Off</sub>	Output current when Off during normal operation	—	10	—	mA	V <sub>in</sub> =0V T <sub>J</sub> =25°C, V <sub>CC</sub> =28V
V <sub>Ih</sub>	Input high threshold voltage	—	1.9	2.2	V	
V <sub>Il</sub>	Input low threshold voltage	1	1.6	—		
I <sub>n hyst.</sub>	Input hysteresis	0.1	0.3	0.5		
I <sub>in, on</sub>	Input current when the part is on	—	15	30	μA	V <sub>in</sub> =5V
V <sub>in, off</sub>	Input voltage when the part is in fault mode	—	0.1	0.4	V	I <sub>in</sub> =5mA

## Switching Electrical Characteristics

V<sub>CC</sub>=28V, Resistive load=2Ω, V<sub>in</sub>=5V, T<sub>J</sub>=25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t <sub>don</sub>	Turn-on delay time to 20%	—	0.9	—	μs	
t <sub>r</sub>	Rise time from 20% to 80% of V <sub>CC</sub>	—	0.3	—		
t <sub>doff</sub>	Turn-off delay time to 80%	—	1.2	—		
t <sub>f</sub>	Fall time from 80% to 20% of V <sub>CC</sub>	—	0.1	—		

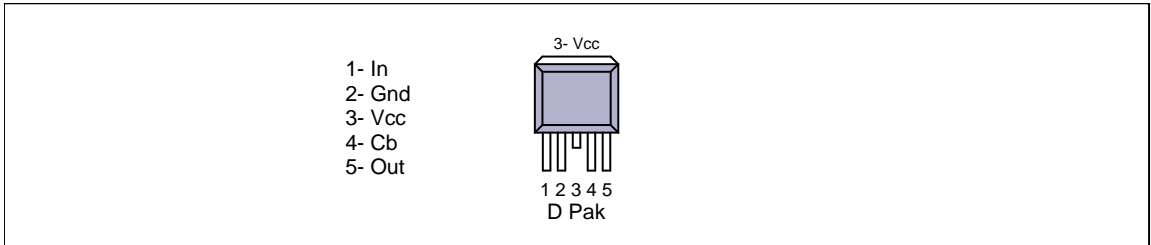
## Protection Characteristics

T<sub>J</sub>=-40..150°C, V<sub>CC</sub>=6..60V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>sd</sub>	Over current shutdown	25	30	45	A	V <sub>out</sub> =0V
T <sub>sd</sub>	Over temperature threshold	150(3)	165	—	°C	
UV H	Under voltage during turn on	—	5	6	V	
UV L	Under voltage during turn off	—	4	5		
T <sub>diag</sub>	Diagnostic time	—	10	—	ms	see figure 1
T <sub>sleep</sub>	Time to enter in sleep mode	7	15	30		see figure 2
T <sub>reset</sub>	Time to enter in sleep mode and reset the fault	—	5	—		see figure 1
T <sub>wkp</sub>	Time to leave the sleep mode	—	0.05	0.5	μs	R <sub>in</sub> =4k7
T <sub>pw on rst</sub>	Power on reset duration	4	8	12		see figure 2 & 3

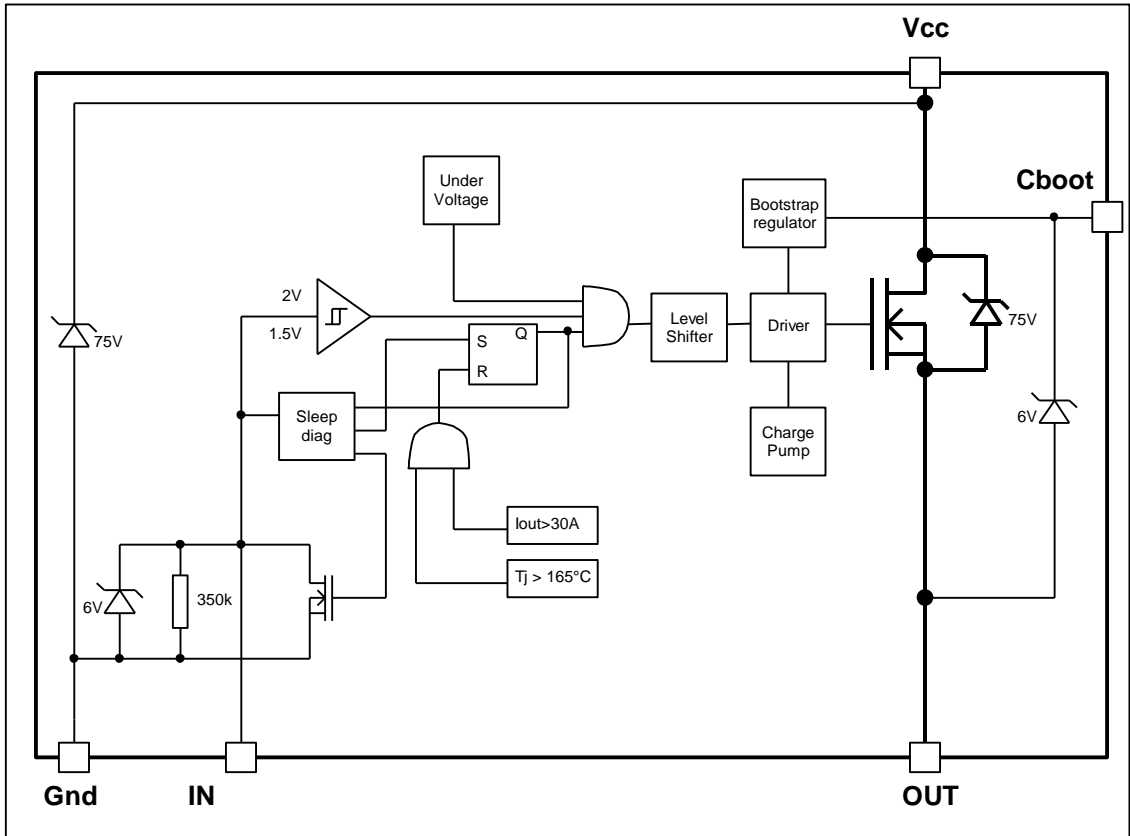
(3) Guaranteed by design

**Lead Assignments**



**Functional Block Diagram**

All values are typical



### Sleep\_mode / Diagnostic

Sleep\_mode block manages the diagnostic and the sleep\_mode. The device enters in sleep mode if input is inactive during a delay higher than  $T_{sleep}$ .

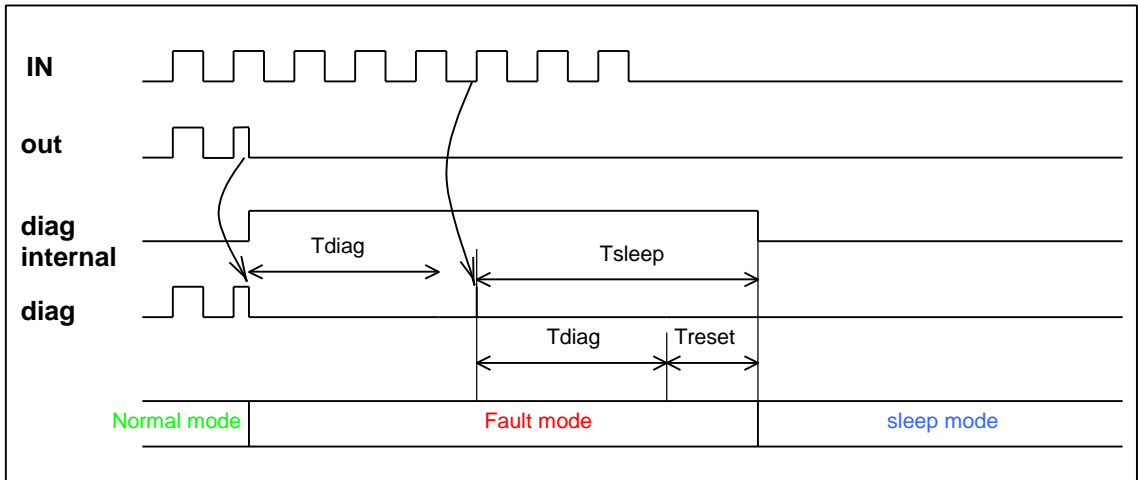
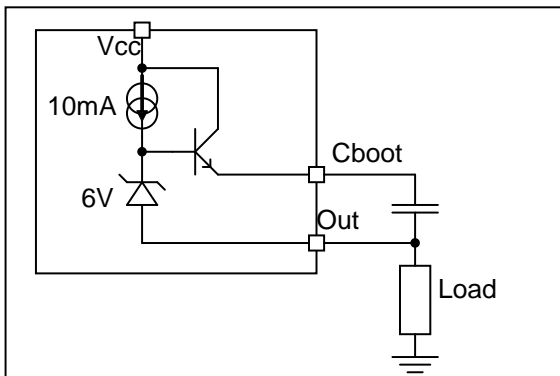


Figure 1

### Bootstrap

The AUIPS7221 integrates a bootstrap regulator to maintain a fixed voltage on the bootstrap capacitor for any battery voltage. The regulator is off during the sleep mode to reduce the current consumption.



The 8mA current source flows permanently on the output when the output is off and the part is not in sleep mode. In case of an open load condition, the output voltage will be at  $V_{cc}-6V$ .

### Wake up sequence

To wake up the part from the sleep mode, the input must be activated at least during  $T_{wkp}$ , then the bootstrap regulator is switched on and the bootstrap capacitor is charged. The output will be not activated during  $T_{pw}$  on rst.

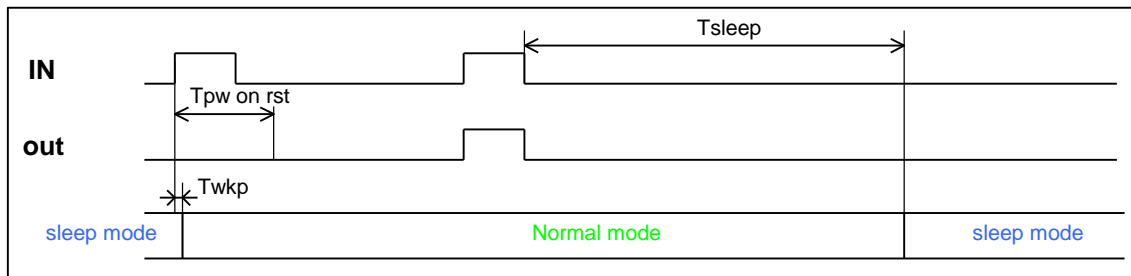


Figure 2

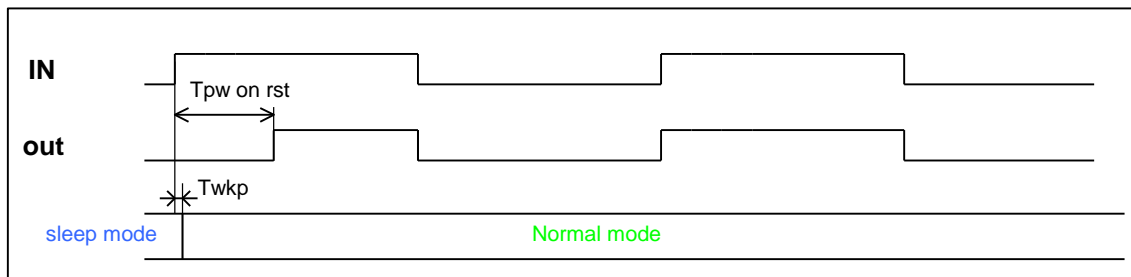
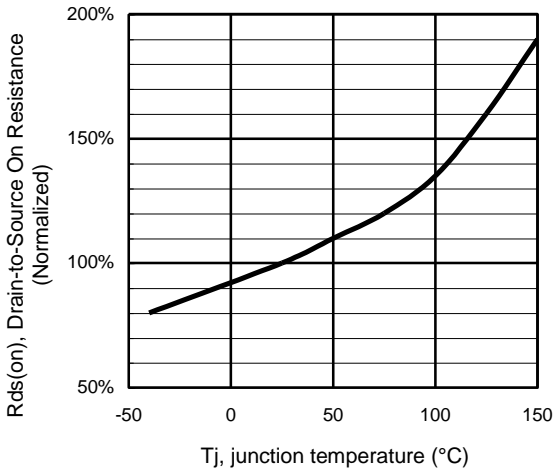
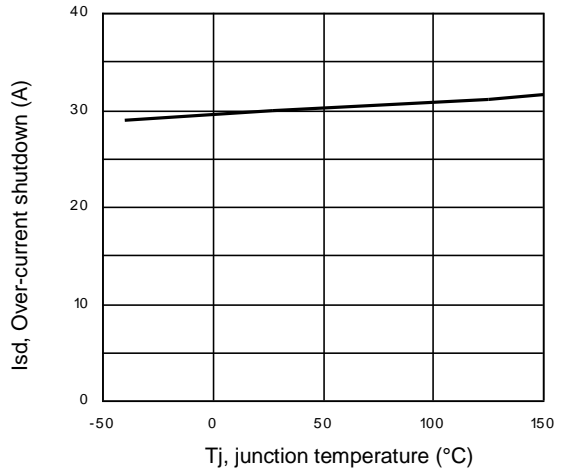


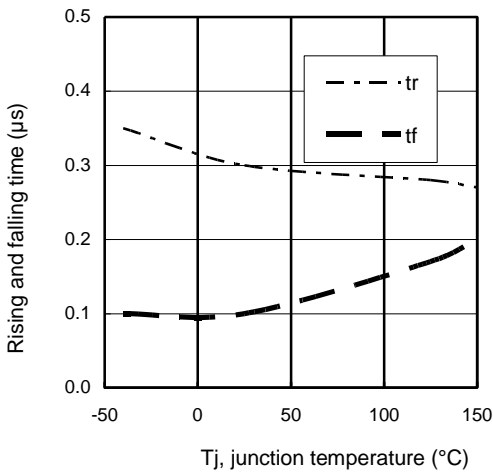
Figure 3



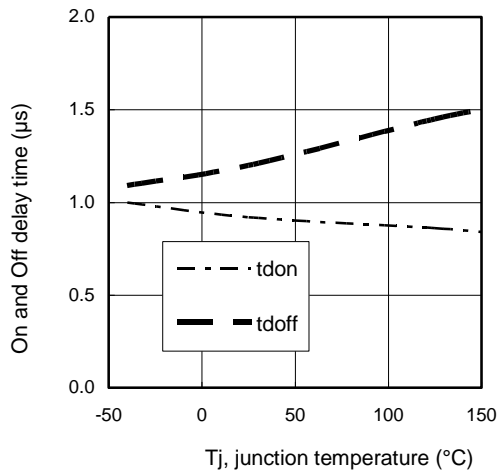
**Figure 5 - Normalized Rds(on) (%) Vs Tj (°C)**



**Figure 6 – Isd (A) Vs Tj (°C)**

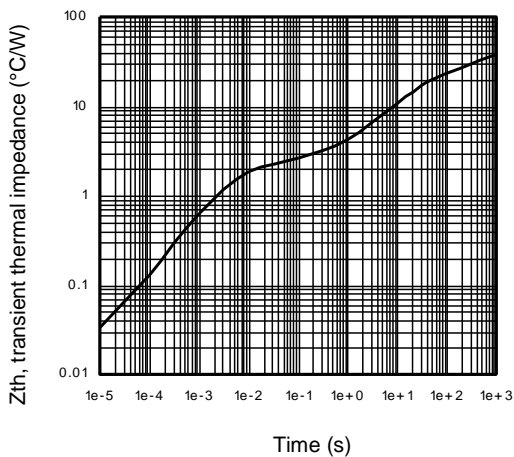


**Figure 7 – tr / tf (µs) Vs Tj (°C)**

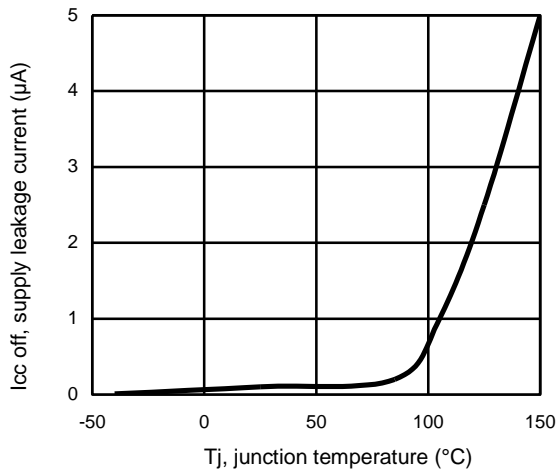


**Figure 8 – tdon / tdoff (µs) Vs Tj (°C)**

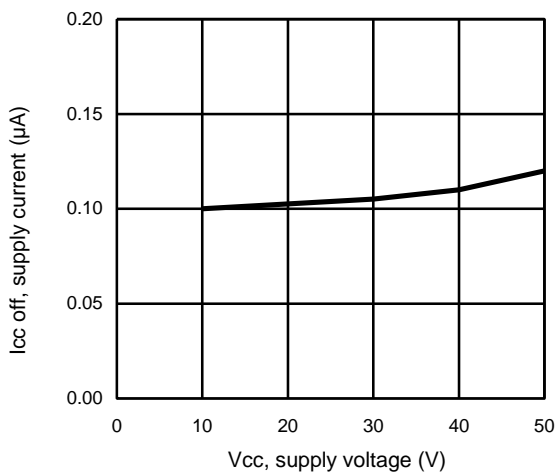




**Figure 9 – Transient thermal impedance (°C/W) Vs time (s)**

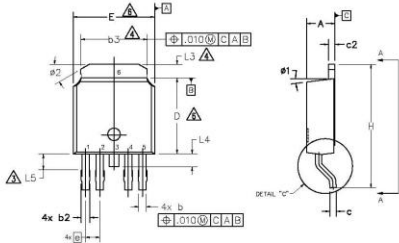
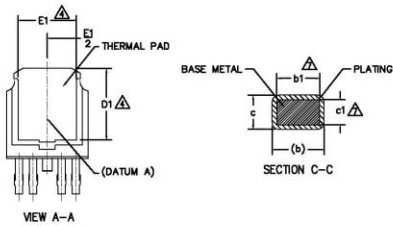
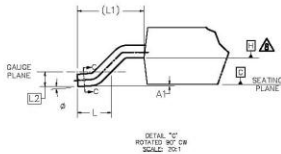


**Figure 10 – I<sub>cc off</sub> (µA) Vs T<sub>j</sub> (°C)**



**Figure 11 – I<sub>cc off</sub>(A) Vs V<sub>cc</sub> (V)**

**Case Outline 5 Lead – DPAK**

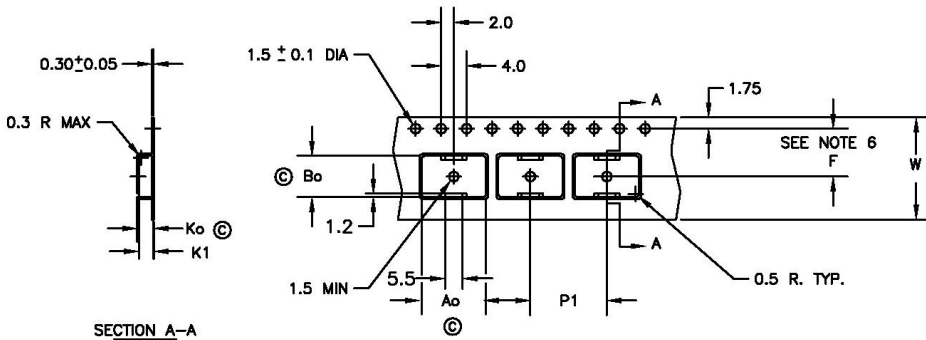


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	—	0.13	—	.005	
b	0.56	0.79	.022	.031	2
b1	.056	0.74	.022	.029	
b2	0.65	0.89	.026	.035	
b3	4.95	5.46	.195	.215	2
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	2
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	—	.205	—	
E	6.35	6.73	.250	.265	3
E1	4.32	—	.170	—	
e	1.14 BSC		.045 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4	—	1.02	—	.040	
L5	1.14	1.52	.045	.060	
φ	0"	10"	0"	10"	
φ1	0"	15"	0"	15"	
φ2	28"	32"	28"	32"	

**NOTES:**

- 1.— DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
- 2.— DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- 3.— LEAD DIMENSION UNCONTROLLED IN L5.
- 4.— DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.— SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.— DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.— DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.— DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.— OUTLINE CONFORMS TO JEDEC OUTLINE TO-252.
10. LEADS AND DRAIN ARE PLATED WITH 100% Sn

**Tape & Reel 5 Lead – DPAK**



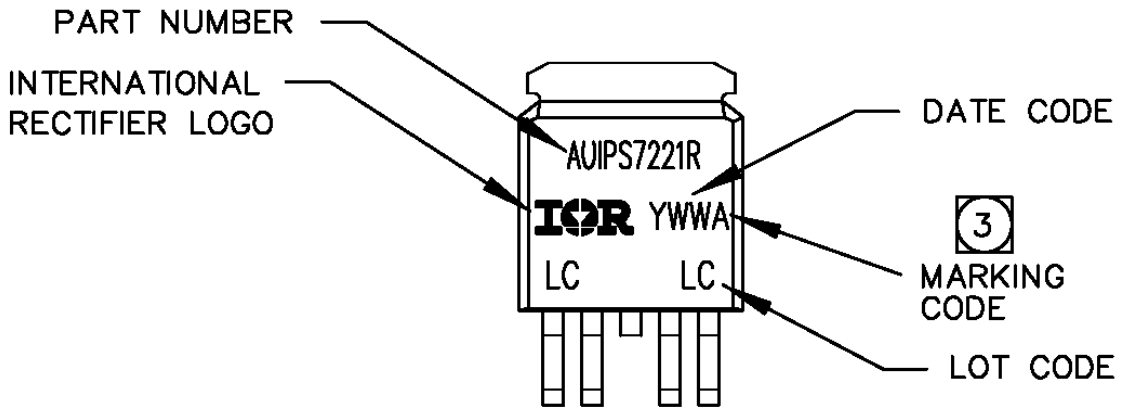
**SECTION A-A**

$A_o = 10.5 \text{ mm}$   
 $B_o = 7.0 \text{ mm}$   
 $K_o = 2.8 \text{ mm}$   
 $K_1 = 2.4 \text{ mm}$   
 $F = 7.5 \text{ mm}$   
 $P_1 = 12.0 \text{ mm}$   
 $W = 16.0 \pm .3 \text{ mm}$

**NOTES:**

1. 10 SPROCKET HOLE PUNCH CUMULATIVE TOLERANCE  $\pm .02$
2. CAMBER NOT TO EXCEED 1mm IN 100mm
3. MATERIAL: CONDUCTIVE BLACK POLYSTYRENE
4.  $A_o$  AND  $B_o$  MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
5.  $K_o$  MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
6. POCKET POSITION RELATIVE TO THE SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
7. VENDOR: (OPTIONAL)
8. MUST ALSO MEET REQUIREMENTS OF EIA STANDARD #EIA-481A, TAPING OF SURFACE-MOUNT COMPONENTS FOR AUTOMATIC PLACEMENT.
9. TOLERANCE TO BE MANUFACTURER STANDARD
10. SURFACE RESISTIVITY OF MOLDED MATL: MUST MEASURE LESS THAN OR EQUAL TO  $10^8$  OHMS PER SQUARE. MEASURED IN ACCORDANCE TO PROCEDURE GIVEN IN ASTM D-257 & ASTM D-991 (REF. C-9000 SPEC.)
11. TOTAL LENGTH PER REEL MUST BE 79 METERS
12. © CRITICAL DIMENSION

## Part Marking Information



## Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIPS7221R	D-Pak-5-Lead	Tube	75	AUIPS7221R
		Tape and reel	2000	AUIPS7221RTR
		Tape and reel left	3000	AUIPS7221RTRL
		Tape and reel right	3000	AUIPS7221RTRR

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### Revision History

<b>Revision</b>	<b>Date</b>	<b>Notes/Changes</b>
A	March, 22nd 2010	Initial release
B	July, 2 <sup>nd</sup> 2010	Update ordering information
C	September, 1 <sup>st</sup> 2011	Update typical schematic page 1
D	February, 21 <sup>st</sup> 2012	Update lout off page 4

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