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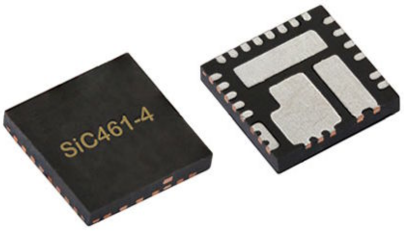
SIC461ED-T1-GE3

Vishay Semiconductors

Buck Switching Regulator IC Positive Adjustable 0.8V 1 Output 10A PowerPAK® MLP55-27

Any questions,please feel free to contact us.
info@kaimte.com

4.5 V to 60 V Input, 2 A, 4 A, 6 A, 10 A microBUCK® DC/DC Converter



LINKS TO ADDITIONAL RESOURCES

PowerCAD Design Tool | Evaluation Boards | Design Tools

DESCRIPTION

The SiC46x is a family of wide input voltage, high efficiency synchronous buck regulators with integrated high side and low side power MOSFETs. Its power stage is capable of supplying high continuous current at up to 2 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.8 V from 4.5 V to 60 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC46x's architecture allows for ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device enables loop stability regardless of the type of output capacitor used, including low ESR ceramic capacitors. The device also incorporates a power saving scheme that significantly increases light load efficiency. The regulator integrates a full protection feature set, including over current protection (OCP), output overvoltage protection (OVP), short circuit protection (SCP), output undervoltage protection (UVP) and over temperature protection (OTP). It also has UVLO for input rail and a user programmable soft start.

The SiC46x family is available in 2 A, 4 A, 6 A, 10 A pin compatible 5 mm by 5 mm lead (Pb)-free power enhanced MLP55-27L package.

TYPICAL APPLICATION CIRCUIT

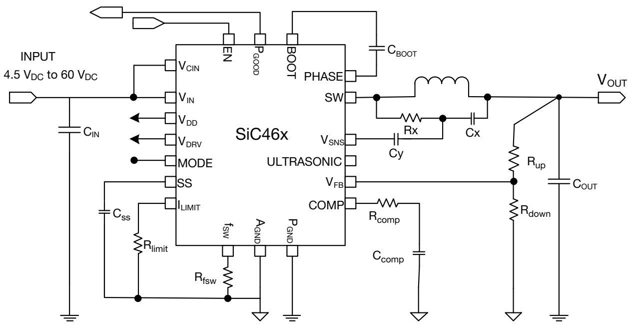


Fig. 1 - Typical Application Circuit for SiC46x

FEATURES

Pb
RoHS
COMPLIANT
HALOGEN
FREE

- Versatile
  - Single supply operation from 4.5 V to 60 V input voltage
  - Adjustable output voltage down to 0.8 V
  - Scalable solution 2 A (SiC464), 4 A (SiC463), 6 A (SiC462), 10 A (SiC461)
  - Output voltage tracking and sequencing with pre-bias start up
  - ± 1 % output voltage accuracy at -40 °C to +125 °C
- Highly efficient
  - 98 % peak efficiency
  - 4 μA supply current at shutdown
  - 235 μA operating current, not switching
- Highly configurable
  - Adjustable switching frequency from 100 kHz to 2 MHz
  - Adjustable soft start and adjustable current limit
  - 3 modes of operation, forced continuous conduction, power save or ultrasonic
- Robust and reliable
  - Output over voltage protection
  - Output under voltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
  - Supported by Vishay PowerCAD online design simulation
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Industrial and automation
- Home automation
- Industrial and server computing
- Networking, telecom, and base station power supplies
- Unregulated wall transformer
- Robotics
- High end hobby electronics: remote control cars, planes, and drones
- Battery management systems
- Power tools
- Vending, ATM, and slot machines

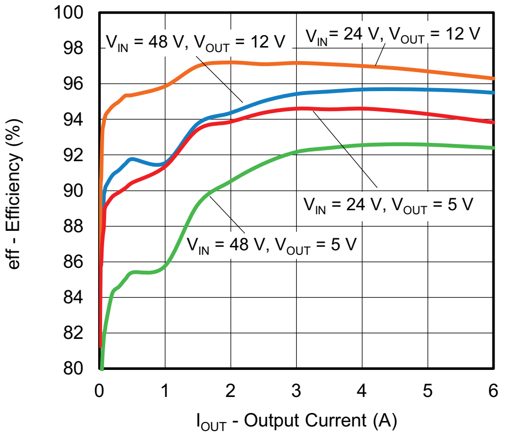


Fig. 2 - SiC462 Efficiency vs. Output Current

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PIN CONFIGURATION

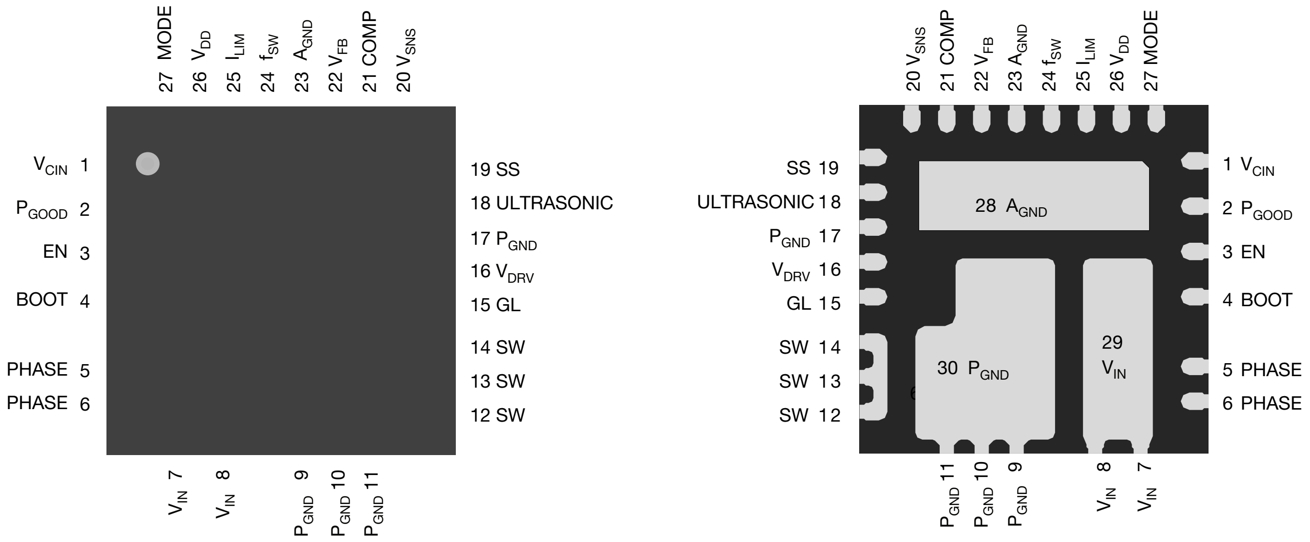

Fig. 3 - SiC46x Pin Configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{CIN}	Supply voltage for internal regulators V_{DD} and V_{DRV}. This pin should be tied to V_{IN}, but can also be connected to a lower supply voltage (> 5 V) to reduce losses in the internal linear regulators
2	P_{GOOD}	Open-drain power good indicator - high impedance indicates power is good. An external pull-up resistor is required
3	EN	Enable pin. Tie high/low to enable/disable the IC accordingly. This is a high voltage compatible pin, can be tied to 60 V
4	BOOT	High side driver bootstrap voltage
5, 6	PHASE	Return path of high side gate driver
7, 8, 29	V_{IN}	Power stage input voltage. Drain of high side MOSFET
9, 10, 11, 17, 30	P_{GND}	Power ground
12, 13, 14	SW	Power stage switch node
15	GL	Low side MOSFET gate signal
16	V_{DRV}	Supply voltage for internal gate driver. When using the internal LDO as a bias power supply, V_{DRV} is the LDO output. Connect a 4.7 µF decoupling capacitor to P_{GND}
18	ULTRASONIC	Float to disable ultrasonic mode, connect to V_{DD} to enable. Depending on the operation mode set by the mode pin, power save mode or forced continuous mode will be enabled when the ultrasonic mode is disabled
19	SS	Set the soft start ramp by connecting a capacitor to A_{GND}. An internal current source will charge the capacitor
20	V_{SNS}	Power inductor signal feedback pin for system stability compensation
21	COMP	Output of the internal error amplifier. The feedback loop compensation network is connected from this pin to the A_{GND} pin
22	V_{FB}	Feedback input for switching regulator used to program the output voltage - connect to an external resistor divider from V_{OUT} to A_{GND}
23, 28	A_{GND}	Analog ground
24	f_{SW}	Set the on-time by connecting a resistor to A_{GND}
25	I_{LIMIT}	Set the current limit by connecting a resistor to A_{GND}
26	V_{DD}	Bias supply for the IC. V_{DD} is an LDO output, connect a 1 µF decoupling capacitor to A_{GND}
27	MODE	Set various operation modes by connecting a resistor to A_{GND}. See specification table for details

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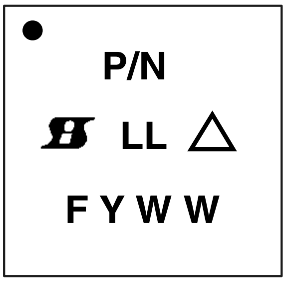
ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING CODE**
SiC461ED-T1-GE3	PowerPAK® MLP55-27L	SiC461
SiC461EVB	Reference board	
SiC462ED-T1-GE3	PowerPAK® MLP55-27L	SiC462
SiC462EVB	Reference board	
SiC463ED-T1-GE3	PowerPAK® MLP55-27L	SiC463
SiC463EVB	Reference board	
SiC464ED-T1-GE3	PowerPAK® MLP55-27L	SiC464
SiC464EVB	Reference board	

PART MARKING INFORMATION



● = pin 1 indicator
P/N = part number code
S = Siliconix logo
△ = ESD symbol
F = assembly factory code
Y = year code
WW = week code
LL = lot code

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMITS**	**UNIT**
V_{CIN}, V_{IN}	Reference to P_{GND}	-0.3 to 66	V
EN	Reference to A_{GND}	-0.3 to 60	
SW / PHASE	Reference to P_{GND}	-0.3 to 66	
V_{DRV}	Reference to P_{GND}	-0.3 to 6	
V_{DD}	Reference to A_{GND}	-0.3 to 6	
SW / PHASE (AC)	Reference to P_{GND}; 100 ns	-10 to 72	
BOOT		-0.3 to V_{PHASE} + V_{DRV}	
A_{GND} to P_{GND}		-0.3 to 0.3	
All other pins	Reference to A_{GND}	-0.3 to V_{DD} + 0.3	
Temperature			
Junction temperature	T_J	-40 to +150	°C
Storage temperature	T_{STG}	-65 to +150	
Power Dissipation			
Thermal resistance from junction-to-ambient		12	°C/W
Thermal resistance from junction-to-case		2	
ESD Protection			
Electrostatic discharge protection	Human body model, JESD22-A114	2000	V
	Charged device model, JESD22-A101	500	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (all voltages referenced to GND = 0 V)				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input voltage (V_{IN})	4.5	-	60	V
Control input voltage (V_{CIN}) (1)	4.5	-	60	
Enable (EN)	0	-	60	
Bias supply (V_{DD})	4.75	5	5.25	
Drive supply voltage (V_{DRV})	4.75	5.3	5.55	
Output voltage (V_{OUT})	0.8	-	0.92 x V_{IN}	
Temperature				
Recommended ambient temperature	-40 to +105			°C
Operating junction temperature	-40 to +125			

Note

(1) For input voltages below 5 V, provide a separate supply to V_{CIN} of at least 5 V to prevent the internal V_{DD} rail UVLO from triggering

ELECTRICAL SPECIFICATIONS ($V_{IN} = V_{CIN} = 48$ V, $V_{EN} = 5$ V, $T_J = -40$ °C to +125 °C, unless otherwise stated)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Power Supplies						
V_{DD} supply	V_{DD}	$V_{IN} = V_{CIN} = 6$ V to 60 V	4.75	5	5.25	V
		$V_{IN} = V_{CIN} = 5$ V	4.7	5	-	
V_{DD} dropout	$V_{DD\_DROPOUT}$	$V_{IN} = V_{CIN} = 5$ V, $I_{VDD} = 1$ mA	-	70	-	mV
V_{DD} UVLO threshold, rising	V_{DD_UVLO}		4	4.25	4.5	V
V_{DD} UVLO hysteresis	$V_{DD\_UVLO\_HYST}$		-	225	-	mV
Maximum V_{DD} current	I_{DD}	$V_{IN} = V_{CIN} = 6$ V to 60 V	3	-	-	mA
V_{DRV} supply	V_{DRV}	$V_{IN} = V_{CIN} = 6$ V to 60 V	4.75	5.3	5.55	V
		$V_{IN} = V_{CIN} = 5$ V	4.8	5	5.2	
V_{DRV} dropout	$V_{DRV\_DROPOUT}$	$V_{IN} = V_{CIN} = 5$ V, $I_{VDD} = 10$ mA	-	160	-	mV
Maximum V_{DRV} current	V_{DRV}	$V_{IN} = V_{CIN} = 6$ V to 60 V	30	-	-	mA
V_{DRV} UVLO threshold, rising	V_{DRV_UVLO}		4	4.25	4.5	V
V_{DRV} UVLO hysteresis	$V_{DRV\_UVLO\_HYST}$		-	295	-	mV
Input current	I_{VCIN}	Non-switching, $V_{FB} > 0.8$ V	-	235	325	μA
Shutdown current	I_{VCIN_SHDN}	$V_{EN} = 0$ V	-	4	8	
Controller and Timing						
Feedback voltage	V_{FB}	$T_J = 25$ °C	796	800	804	m/V
		$T_J = -40$ °C to +125 °C (1)	792	800	808	
V_{FB} input bias current	I_{FB}		-	2	-	nA
Transconductance	g_m		-	0.3	-	mS
COMP source current	I_{COMP_SOURCE}		15	20	-	μA
COMP sink current	I_{COMP_SINK}		15	20	-	
Minimum on-time	$t_{ON\_MIN.}$		-	90	110	ns
t_{ON} accuracy	$t_{ON\_ACCURACY}$		-10	-	10	%
On-time range	t_{ON_RANGE}		110	-	8000	ns
Frequency range	f_{sw}	Ultrasonic mode enabled	20	-	2000	kHz
		Ultrasonic mode disabled	0	-	2000	
Minimum off-time	$t_{OFF\_MIN.}$		190	250	310	ns
Soft start current	I_{SS}		3	5	7	μA
Soft start voltage	V_{SS}	When V_{OUT} reaches regulation	-	1.5	-	V

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ELECTRICAL SPECIFICATIONS ($V_{IN} = V_{CIN} = 48$ V, $V_{EN} = 5$ V, $T_J = -40$ °C to +125 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fault Protections						
Valley current limit	I_{OCP}	SiC461 (10 A), $R_{ILIM} = 60$ kΩ, $T_J = -10$ °C to +125 °C	10.4	13	15.6	A
		SiC462 (6 A), $R_{ILIM} = 60$ kΩ, $T_J = -10$ °C to +125 °C	6.4	8	9.6	
		SiC463 (4 A), $R_{ILIM} = 40$ kΩ, $T_J = -10$ °C to +125 °C (2)	4.8	6	7.2	
		SiC464 (2 A), $R_{ILIM} = 60$ kΩ, $T_J = -10$ °C to +125 °C	3.2	4	4.8	
Output OVP threshold	V_{OVP}	V_{FB} with respect to 0.8 V reference	-	20	-	%
Output UVP threshold	V_{UVP}		-	-80	-	
Over temperature protection	T_{OTP_RISING}	Rising temperature	-	150	-	°C
	T_{OTP_HYST}	Hysteresis	-	35	-	
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.8 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.8 V reference	-	-10	-	
Power good hysteresis	V_{FB_HYST}		-	50	-	mV
Power good on resistance	R_{ON_PGOOD}		-	7.5	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	μs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		-	1.35	-	V
EN logic low level	V_{EN_L}		-	1.2	-	
EN hysteresis	V_{HYST}		-	0.15	-	
EN pull down resistance	R_{EN}		-	5	-	MΩ
Ultrasonic mode high Level	$V_{ULTRASONIC\_H}$		2	-	-	V
Ultrasonic mode low level	$V_{ULTRASONIC\_L}$		-	-	0.8	
Mode pull up current	I_{MODE}		3.75	5	6.25	μA
Mode 1	R_{MODE}	Power save mode enabled, V_{DD}, V_{DRV} Pre-reg on	0	2	100	kΩ
Mode 2		Power save mode disabled, V_{DD}, V_{DRV} Pre-reg on	298	301	304	
Mode 3		Power save mode disabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	494	499	504	
Mode 4		Power save mode enabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	900	1000	1100	

Notes

[1] Guaranteed by design

[2] Guaranteed by design for SiC463 OCP measurements

FUNCTIONAL BLOCK DIAGRAM

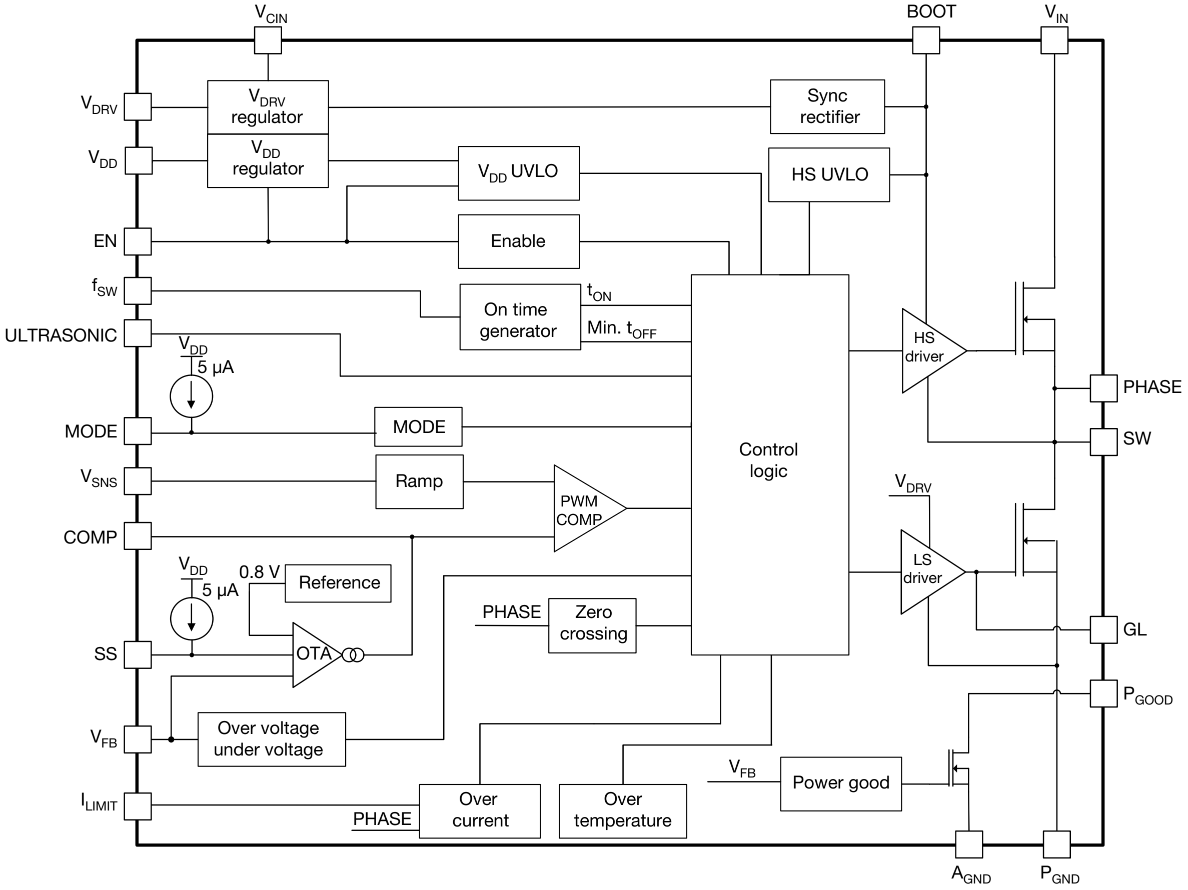

Fig. 4 - SiC46x Functional Block Diagram

OPERATIONAL DESCRIPTION

Device Overview

SiC46x is a high efficiency synchronous buck regulator family capable of delivering up to 10 A continuous current. The device has programmable switching frequency of 100 kHz to 2 MHz. The voltage mode, constant on time control scheme delivers fast transient response, minimizes the number of external components and enables loop stability regardless of the type of output capacitor used, including low ESR ceramic capacitors. The device also incorporates a power saving feature that enables diode emulation mode and frequency fold back as the load decreases.

SiC46x has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output overvoltage protection
- Output undervoltage protection with auto retry
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output
- This device is available in MLP55-27L package to deliver high power density and minimize PCB area

Power Stage

SiC46x integrates a high performance power stage with a n-channel high side MOSFET and a n-channel low side MOSFET optimized to achieve up to 98 % efficiency.

The power input voltage (V_{IN}) can go up to 60 V and down as low as 4.5 V for power conversion.

Control Scheme

SiC46x employs a voltage mode COT control mechanism in conjunction with adaptive zero current detection which allows for power saving in discontinuous conduction mode (DCM). The switching frequency, f_{SW}, is set by an external resistor to A_{GND}, R_{fsw}. The SiC46x operates between 100 kHz to 2 MHz depending on V_{IN} and V_{OUT} conditions.

$$R_{fsw} = \frac{V_{OUT}}{f_{sw} \times 190 \times 10^{-12}}$$

Note, as long as V_{IN} and V_{CIN} are connected together, f_{SW} has no dependency on V_{IN} as the on time is adjusted as V_{IN} varies. During steady-state operation, feedback voltage (V_{FB}) is compared with internal reference (0.8 V typ.) and the amplified error signal (V_{COMP}) is generated at the comp node by the external compensation components, R_{COMP} and C_{COMP}. An externally generated ramp signal and V_{COMP} feed into a comparator. Once V_{RAMP} crosses V_{COMP}, an on-time

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pulse is generated for a fixed time. During the on-time pulse, the high side MOSFET will be turned on. Once the on-time pulse expires, the low side MOSFET will be turned on after a dead time period. The low side MOSFET will stay on for a minimum duration equal to the minimum off-time ($t_{OFF\_MIN.}$) and remains on until V_{RAMP} crosses V_{COMP}. The cycle is then repeated.

Fig. 6 illustrates the basic block diagram for voltage mode, constant on time architecture with external ripple injection, V_{RAMP}, while Fig. 5 illustrates the basic operational principle.

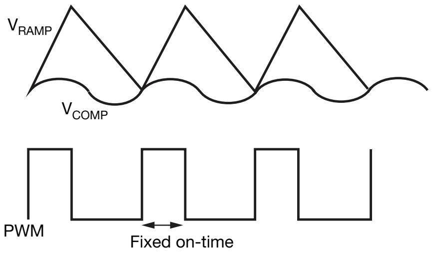

Fig. 5 - SiC46x Operational Principle

The need for ripple injection in this architecture is explained below. First, let us understand the basic principles of this control architecture:

- The reference of a basic voltage mode COT regulator is replaced with a high gain error amplifier loop. The loop ensures the DC component of the output voltage follows the internal accurate reference voltage, providing excellent regulation
- A second voltage feedback path via V_{SNS} with a V_{RAMP} scheme ensures rapid correction of the transient perturbation
- This establishes two voltage loops, one is the steady state voltage feedback path (via the FB pin) and the other is the feed forward path (via the V_{SNS} pin). The scheme gives the user the fast transient response of a COT regulator and the stable, jitter free, line and load regulation performance of a PWM controller

Choosing the Ripple Injection Component Values

For stability purposes the SiC46x requires adequate ripple injection amplitude. Adequate ripple amplitude is required for two main reasons:

1. To reduce jitter due to noise coupled into the system
2. To provide stable operation. Sub harmonic oscillation can occur with constant on time ripple control if below condition is not met

$$ESR \times C_{OUT} > \frac{t_{ON}}{2}$$

Therefore, when the converter design uses an all ceramic output capacitor or other low ESR output capacitors, instability can occur. In order to avoid this, a V_{RAMP} network is used to increase the equivalent R_{ESR} in order to satisfy the above condition. The V_{RAMP} amplitude must be large enough to avoid instability or noise sensitivity but not too large that it degrades transient performance. To ensure stable operation under CCM, DCM and ultrasonic mode, minimum V_{RAMP} amplitude of 100 mV is recommended for the SiC46x family of regulators. A maximum V_{RAMP} of 900 mV is recommended so as not to degrade transient response.

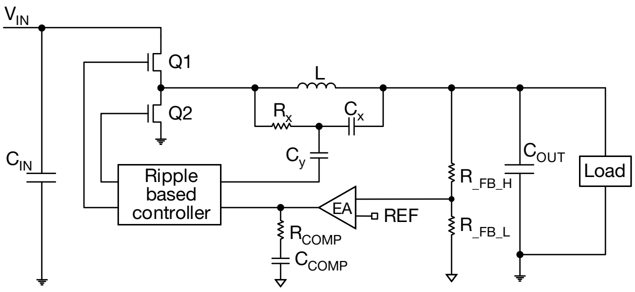

Fig. 6 - SiC46x Control Block Diagram

Below is the equation for calculating the V_{RAMP} amplitude.

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{(V_{IN} \times f_{sw} \times C_x \times R_x)}$$

V_{RAMP} amplitude is a function of V_{IN}, V_{OUT}, and switching frequency and should be adjusted whenever V_{IN}, V_{OUT}, or switching frequency is changed.

For a given buck regulator design, V_{OUT} and switching frequency is typically fixed, while the converter may be expected to work for a wide V_{IN} range. The V_{RAMP} amplitude will increase as V_{IN} is increased and increase the power dissipated by R_X. A proper selection of R_X, package size and value, should take into account the maximum power dissipation at the expected operating conditions.

In order to optimize the V_{RAMP} amplitude over a desired V_{IN} range use the following procedure to calculate R_x, C_x, and C_y.

1. The equation below calculates R_X as a function of V_{IN}, V_{OUT}, and maximum allowable power dissipated by R_X.

   $$R_x = \frac{V_{IN\_MAX.} \times V_{OUT} \times (1 - D)}{P_{RX\_MAX.}}$$

   where $P_{RX\_MAX.}$ is the maximum allowed power dissipation in R_x. Note, the maximum power dissipation of a 0603 sized resistor is typically 25 mW. Power dissipation derating must be taken into account for high ambient temperatures
2. The equation below calculates $C_{X\_MIN.}$ as a function of V_{IN} and maximum allowed V_{RAMP} amplitude.

   $$C_{X\_MIN.} = \frac{P_{RX\_MAX.}}{V_{IN\_MAX.} \times f_{sw} \times V_{RAMP\_MAX.}}$$

   where $V_{RAMP\_MAX.}$ = 900 mV
3. Using V_{RAMP} equation, calculate $V_{RAMP\_MIN.}$ at minimum V_{IN} based on the R_x and the minimum C_x value calculated above
4. If $V_{RAMP\_MIN.}$ is > 200 mV, set C_x to $C_{X\_MIN.}$, otherwise set C_x to ($C_{x\_MIN.}$ x $V_{RAMP\_MIN.}$/200 mV). If $V_{RIPPLE\_MIN.}$ is < 100 mV, increase $P_{RX\_MAX.}$ and recalculate R_X and C_X
5. C_y should be large enough not to distort the V_{RAMP} and small enough not to load excessively the V_{RAMP} network (R_x and C_x). Please use the follow formula: $C_y = 1/(820 \times f_{sw})$

This procedure allows for a maximum range of operation.

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Error Amplifier Compensation Value Selection (for reference only)

R_{COMP} and C_{COMP} in the Fig. 6 are the components used to compensate the control loop.

For optimal transient response, the crossover frequency should be:

- Set typically at 1/10th to 1/5th of the converter switching frequency (Vishay's component calculator tool uses 1/10th the converter switching frequency)
- Be above the LC filter resonance frequency which is $1/2\,\pi\sqrt{LC}$

The procedure to select the R_{COMP} and C_{COMP} such that the above conditions are met is as follows:

1. Plot the magnitude and phase of the control to output transfer function using the equation below.
   Control to output transfer function.

$$H(s) = A \times \frac{1 + sR_C C_o \times (1 + sR_x C_x) \times (1 + sR_y C_y)}{\left(1 + \frac{sL}{R_o} + s^2 LC_o\right) \times (1 + sR_x C_x) \times (1 + sR_y C_y) + AR_y C_y s \times \left[1 + s \times \left(R_x C_x + \frac{L}{R_o}\right) + s^2 \times (R_x R_c C_x C_o + LC_o)\right]}$$

   Where $A = (2V_{IN} \times R_x \times C_x \times f)/V_{OUT}$, R_x, C_x, C_y are components for ripple injection as shown in Fig. 6 and R_y is the internal impedance of the V_{SNS} pin and is = 65 kΩ.
   C_o - output capacitance
   R_c - output capacitor ESR

2. From the plot of the control to output transfer function, determine the gain and phase at the crossover frequency

3. Calculate the R_{COMP} using the equation

$$R_{COMP} = \frac{1}{G_H \times gm \times r_{FB}}$$

   where G_H is the gain of the transfer function at cross over frequency, "g_m" is the transconductance of the error amplifier (300 μS) and r_{FB} is the ratio of the feedback divider, r_{FB} = R_FB_L/(R_FB_L + R_FB_H)

4. Select C_{COMP} based on the placement of the zero such that phase margin is sufficient at the cross over frequency. A phase margin of over 60° is sufficient for converter stability. A good starting point is to place the compensation zero at 1/5th of the LC pole

$$C_{COMP} = \frac{5\sqrt{LC}}{R_{COMP}}$$

Once the component values are calculated, it is now possible to calculate the total loop gain. The total loop gain is the product of the control to output transfer function and the error amplifier transfer function.

The transfer function of the error amplifier is given by the equation below.

$$G(s) = gmR_o \times \frac{(1 + sR_{COMP}C_{COMP}) \times r_{FB}}{(1 + s \times (R_{COMP}C_{COMP} + R_o C_{COMP}))}$$

Where R_o = 40 MΩ is the output resistance of the transconductance amplifier.
Total loop transfer function = H(s)G(s)

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Power-Save Mode, Mode Pin, and Ultrasonic Pin Operation

To improve efficiency at light-loads, SiC46x provides a set of innovative implementations to reduce low side re-circulating current and switching losses. The internal zero crossing detector monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor current crosses zero, the device first deploys diode mode by turning off the low side MOSFET. If load further decreases, switching frequency is reduced proportional to the load condition to save switching losses while keeping output ripple within tolerance. If the ultrasonic pin is tied to V_{DD}, the minimum switching frequency in discontinuous mode is > 20 kHz to avoid switching frequencies in the audible range. If this feature is not required ultrasonic mode can be disabled by floating the ULTRASONIC pin. When ultrasonic mode is disabled, the regulator will operate in forced continuous mode or power save mode where there is no limit to the lower frequency limit. In this state, at zero load, switching frequency can go as low as hundreds of hertz.

To improve the converter efficiency, the user can choose to disable the internal V_{DRV} regulator by picking either mode 3 or mode 4 and connecting a 5 V supply to the V_{DRV} pin. This reduces power dissipation in the SiC46x by eliminating the V_{DRV} linear regulator losses.

The mode pin supports several modes of operation as shown in table 1. An internal current source is used to set the voltage on this pin using an external resistor:

TABLE 1 - OPERATION MODES

MODE	RANGE (kΩ)	POWER SAVE MODE	INTERNAL V_{DRV} REGULATOR
1	0 to 100	Enabled	ON
2	298 to 304	Disabled	ON
3	494 to 504	Disabled	OFF [1]
4	900 to 1100	Enabled	OFF [1]

Note

[1] Connect a 5 V (± 5 %) supply to the V_{DRV} pin

The mode pin is not latched to any state and can be changed on the fly.

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiC46x has pulse-by-pulse over current limit control. The inductor current is monitored during low side MOSFET conduction time through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the inductor current is compared with an internal OCP threshold. If inductor current is higher than OCP threshold, high side MOSFET is kept off until the inductor current falls below OCP threshold.

OCP is enabled immediately after V_{DD} passes UVLO level.

OCP is set by an external resistor, R_{LIM} to A_{GND}. (See table 2)

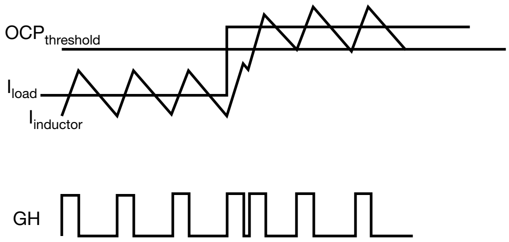

Fig. 7 - Over-Current Protection Illustration

Output Undervoltage Protection (UVP)

UVP is implemented by monitoring the FB pin. If the voltage level at FB drops below 0.16 V for more than 25 μs, a UVP event is recognized and both high side and low side MOSFETs are turned off. After a duration equivalent to 20 soft start periods, the IC attempts to re-start. If the fault condition still exists, the above cycle will be repeated.

UVP is only active after the completion of soft-start sequence.

Output Over Voltage Protection (OVP)

OVP is implemented by monitoring the FB pin. If the voltage level at FB rising above 0.96 V, a OVP event is recognized and both high side and low side MOSFETs are turned off. Normal operation is resumed once FB voltage drop below 0.91 V.

Over Temperature Protection (OTP)

OTP is implemented by monitoring the junction temperature. If the junction temperature rises above 150 °C, a OTP event is recognized and both high side and low MOSFETs are turned off. After the junction temperature falls below 115 °C (35 °C hysteresis), the device restarts by initiating a soft start sequence.

Sequencing of Input / Output Supplies

SiC46x has no sequencing requirements on its supplies or enables (V_{IN}, V_{CIN}, V_{DD}, V_{DRV}, EN).

Enable

The SiC46x has an enable pin to turn the part on and off. Driving this pin above 1.35 V enables the device, while driving the pin below 1.2 V disables the device.

The EN pin is internally pulled to A_{GND} by a 5 MΩ resistor to prevent unwanted turn on due to a floating GPIO.

Soft-Start

During soft start time period, inrush current is limited and the output voltage is ramped gradually. The following control scheme is implemented:

Once the V_{DD} voltage reaches the UVLO trip point, an internal “Soft start Reference” (SR) begins to ramp up. The SR ramp rate is determined by the external soft start capacitor and an internal 5 μA current source tied to the soft start pin.

The internal SR signal is used as a reference voltage to the error amplifier (see functional block diagram). The control scheme guarantees that the output voltage during the soft start interval will ramp up coincidently with the SR voltage. The soft-start time, t_{SS}, is adjustable by calculating a capacitor value from the following equation.

$$t_{ss} = \frac{C_{ss} \text{ x } 0.8 \text{ V}}{5 \text{ μA}}$$

During soft-start period, OCP is activated. Short circuit protection is not active until soft-start is complete.

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Pre-Bias Start-Up

In case of pre-bias startup, output is monitored through FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents high side and low side MOSFETs from switching to avoid negative output voltage spike and excessive current sinking through low side MOSFET.

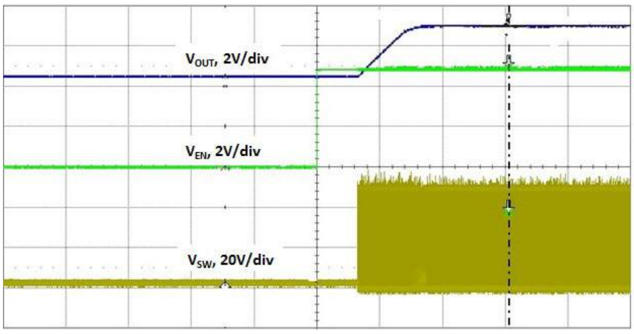


Fig. 8 - Pre-Bias Start-Up

Power Good

SiC46x's power good is an open-drain output. Pull P_{GOOD} pin high through a > 10K resistor to use this signal. Power good window is shown in Fig. 9. If voltage on FB pin is out of this window, P_{GOOD} signal is de-asserted by pulling down to A_{GND}. To prevent false triggering during transient events, P_{GOOD} has a 25 μs blanking time.

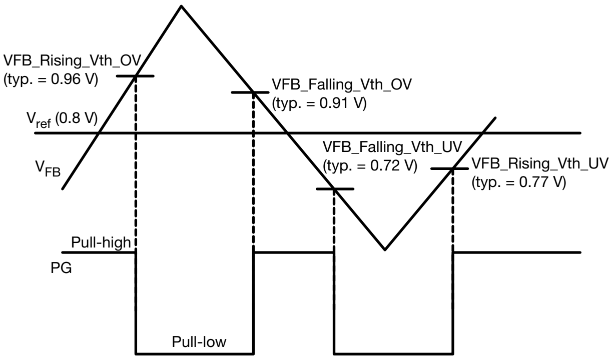
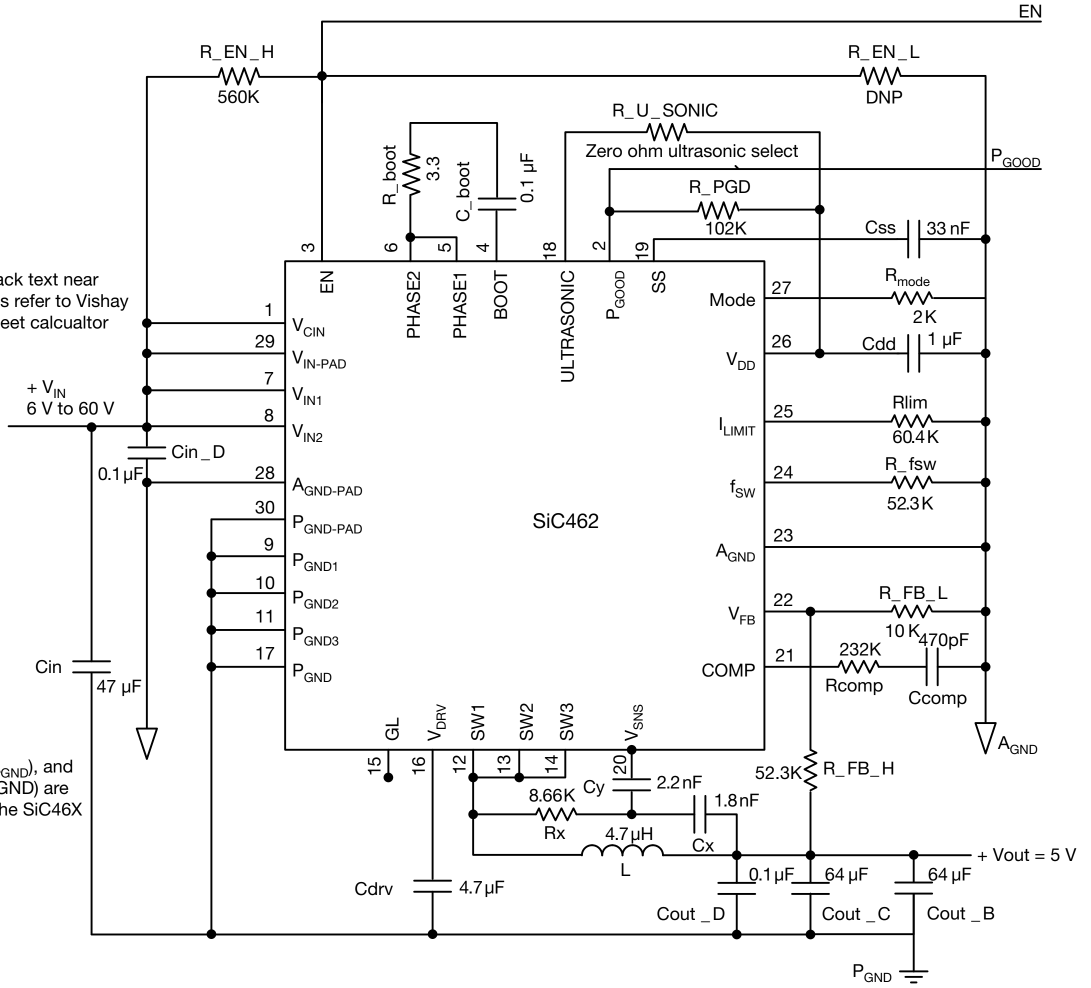


Fig. 9 - P_{GOOD} Window

EXAMPLE SCHEMATIC OF SiC462



Notes in small black text near component values refer to Vishay SiC46X spreadsheet calcualtor references

Analog ground (A_{GND}), and power ground (PGND) are tied internally in the SiC46X

Fig. 10 - SiC462 Configured for 6 V to 60 V Input, 5 V Output at 6 A, 500 kHz Operation with Ultrasonic Power Save Mode Enabled all Ceramic Output Capacitance Design

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EXTERNAL COMPONENT SELECTION FOR THE SiC46x

This section explains external component selection for the SiC46x family of regulators. Component reference designators in any equation refer to the schematic shown in Fig. 10.

The online simulation tool PowerCAD helps to make external component calculation simple. The user simply needs to enter required operating conditions.

Output Voltage Adjustment

If a different output voltage is needed, simply change the value of V_{OUT} and solve for $R_{\_FB\_H}$ based on the following formula:

$$R_{\_FB\_H} = \frac{R_{\_FB\_L}(V_{OUT} - V_{FB})}{V_{FB}}$$

where V_{FB} is 0.8 V. $R_{\_FB\_L}$ should be a maximum of 10 kΩ to prevent V_{OUT} from drifting at no load.

Switching Frequency Selection

The following equation illustrates the relationship between frequency, V_{IN}, V_{OUT}, and R_{fsw} value:

$$R_{fsw} = \frac{V_{OUT}}{f_{sw} \times (190 \times 10^{-12})}$$

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values allow for the use of smaller package sizes but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current and, for a given DC resistance, are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power save operation. The SiC46x will typically enter power save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 1.8 A, power save operation will be active for loads less than 0.9 A. If ripple current is set at 30 % of maximum load current, power save will typically start at a load which is 15 % of maximum current.

The inductor value is typically selected to provide ripple current of 25 % to 50 % of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance. During the on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equations for determining inductance are shown below.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{sw}}$$

and

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{OUT\_MAX.} \times K}$$

where, K is the maximum percentage of ripple current. The designer can quickly make a choice of inductor if the ripple percentage is decided, usually no more than 30 % however higher or lower percentages of I_{OUT} can be acceptable depending on application. This device allows choices larger than 30 %.

Other than the inductance the DCR and saturation current parameters are key values. The DCR causes an I^2R loss which will decrease the system efficiency and generate heat. The saturation current has to be higher than the maximum output current plus ½ of the ripple current. In an over current condition the inductor current may be very high. All this needs to be considered when selecting the inductor.

Output Capacitor Selection

The SiC46x is stable with any type of output capacitors by choosing the appropriate V_{RAMP} components. This allows the user to choose the output capacitance based on the best trade off of board space, cost and application requirements.

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple voltage requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus half of the peak-to-peak ripple. A change in the output ripple voltage will lead to a change in DC voltage at the output. The relationship between output voltage ripple, output capacitance and ESR of the output capacitor is shown by the following equation:

$$V_{RIPPLE} = I_{RIPPLE(MAX.)} \times \left(\frac{1}{8 \times C_o \times f_{sw}} + ESR\right) \quad (1)$$

Where V_{RIPPLE} is the maximum allowed output ripple voltage; $I_{RIPPLE(MAX.)}$ is the maximum inductor ripple current; f_{sw} is the switching frequency of the converter; C_o is the total output capacitance; ESR is the equivalent series resistance of the total output capacitors.

In addition to the output ripple voltage requirement, the output capacitors need to meet transient requirements. A worst case load release condition (from maximum load to no load at the exact moment when inductor current is at the peak) determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero within 1 μs), the output capacitor must absorb all the energy stored in the inductor. The peak voltage on the capacitor, V_{PK}, under this worst case condition can be calculated by following equation:

$$C_{OUT\_MIN.} = \frac{L \times \left(I_{OUT} + \frac{1}{2} \times I_{RIPPLE(MAX.)}\right)^2}{(V_{PK})^2 - (V_{OUT})^2} \quad (2)$$

During the load release time, the voltage across the inductor is approximately $-V_{OUT}$. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the di/dt of the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor; therefore a smaller capacitance can be used. The following can be used to calculate the required capacitance for a given di_{LOAD}/dt.

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Peak inductor current, I_{LPK}, is shown by the next equation:

$$I_{LPK} = I_{MAX.} + \frac{1}{2} \times I_{RIPPLE(MAX.)}$$

The slew rate of load current = $\frac{di_{LOAD}}{dt}$

$$C_{OUT\_MIN.} = I_{LPK} \times \frac{L \times \left(\frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX.}}{dI_{LOAD}} \times dt \right)}{2(V_{PK} - V_{OUT})} \qquad (3)$$

Based on application requirement, either equation (2) or equation (3) can be used to calculate the ideal output capacitance to meet transition requirement. Compare this calculated capacitance with the result from equation (1) and choose the larger value to meet both ripple and transition requirement.

Enable Pin Voltage

The EN pin has an internal 5 MΩ pull down resistor connected to A_{GND}. In order to enable the device, an external signal greater than 1.4 V is required. The enable can also be used to set the minimum V_{CIN}, V_{IN} startup voltage by connecting a voltage divider between V_{IN}, EN, and P_{GND}. An automated calculator is available to assist in component selection.

Current Limit Resistor

The current limit is set by placing a resistor between I_{LIM} and A_{GND}. The values can be found using the following equation:

$$R_{LIM}\,(k\Omega) = \frac{K_{LIM}}{I_{OUT\_MAX.} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times f_{sw} \times V_{IN} \times L}}$$

Where

- $I_{OUT\_MAX.}$ is desired DC current limit level
- K_{LIM} is determined by Table 2

TABLE 2 - K_{LIM} VALUE

PART NUMBER	K_{LIM}
SiC461	780K
SiC462	480K
SiC463	240K
SiC464	240K

Note

- It is suggested that the current limit setting not be higher than 2 times the rated current of the part. Be sure max. current limit is within the saturation current of the inductor

Input Capacitance

In order to determine the minimum capacitance the input voltage ripple needs to be specified; $V_{IN\_PK-PK} \leq 500$ mV is a suitable starting point. This magnitude is determined by the final application specification. The input current needs to be determined for the lowest operating input voltage,

$$I_{VCIN(RMS)} = I_O \times \sqrt{D \times (1 - D) + \frac{1}{12} \times \left(\frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}} \right)^2 \times (1 - D)^2 \times D}$$

The minimum input capacitance can then be found,

$$C_{VIN\_MIN.} = I_{OUT} \times \frac{D \times (1 - D)}{V_{IN\_PK-PK} \times f_{sw}}$$

If high ESR capacitors are used, it is good practice to also add low ESR ceramic capacitance. A 4.7 µF ceramic input capacitance is a suitable starting point.

Note, account for voltage derating of capacitance when using all ceramic input capacitors.

Efficiency Measurement

Fig. 11 to 39 in the following pages are the efficiency data for the SiC461, SiC462, SiC463, and SiC464.

The measurements are taken based on the Vishay 6 layers, 2 ounce copper evaluation board.

The inductors used in the measurement are tabulated below.

TABLE 3 - INDUCTOR VALUES

DEVICE PART	INDUCTANCE (µH)	INDUCTOR PART NUMBER	DCR (mΩ)
SiC461	3.3	IHLP6767GZER3R3M11	2.79
	4.7	IHLP6767GZER4R7M11	3.98
	6.8	IHLP6767GZER6R8M11	5.86
	8.2	IHLP6767GZER8R2M11	7.71
	10	IHLP6767GZER100M11	8.89
SiC462	5.6	IHLP5050FDER5R6M51	8.51
	6.8	IHLP5050FDER6R8M51	11.30
	8.2	IHLP5050FDER8R2M51	13.20
	10	IHLP5050FDER100M51	16.60
	15	IHLP5050FDER150M51	24.00
SiC463	10	IHLP5050FDER100M51	16.60
	15	IHLP5050FDER150M51	24.00
	22	IHLP5050FDER220M51	31.30
SiC464	10	IHLP5050FDER100M51	16.60
	15	IHLP5050FDER150M51	24.00
	22	IHLP5050FDER220M51	31.30

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC461 (10 A), unless otherwise noted)

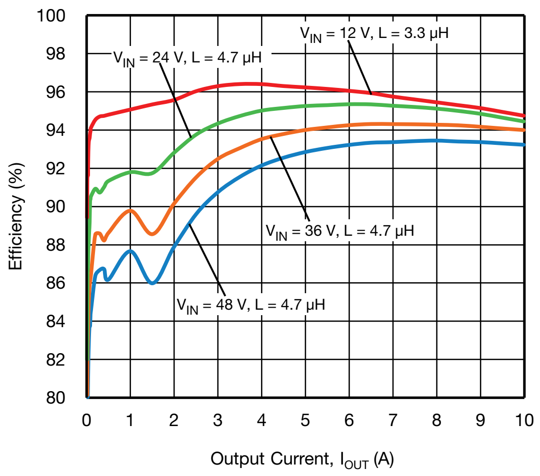

Fig. 11 - SiC461 Efficiency vs. Output Current, V_{OUT} = 5 V

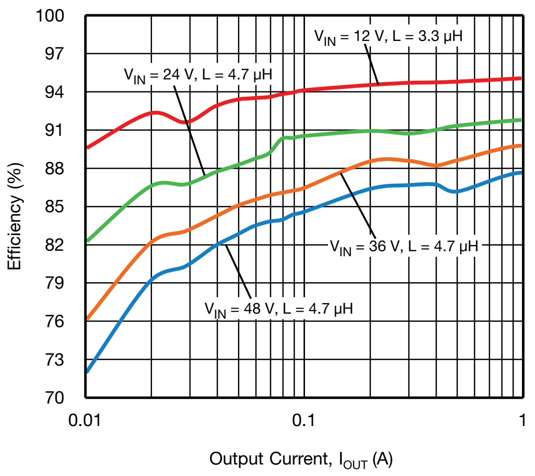

Fig. 14 - SiC461 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

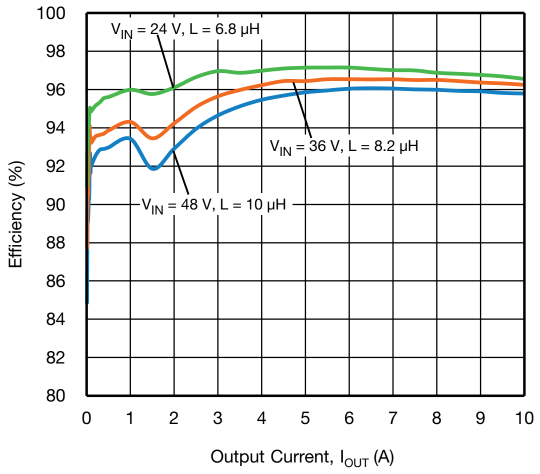

Fig. 12 - SiC461 Efficiency vs. Output Current, V_{OUT} = 12 V

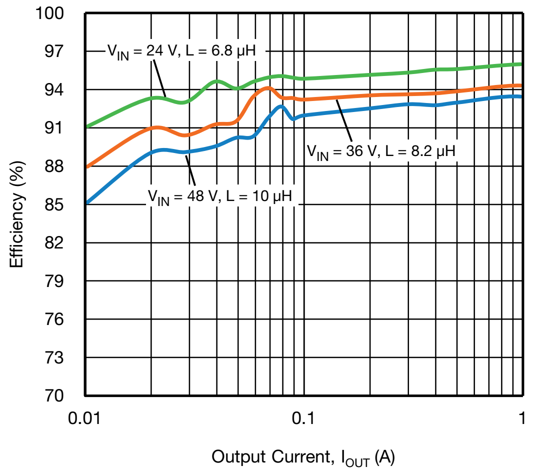

Fig. 15 - SiC461 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

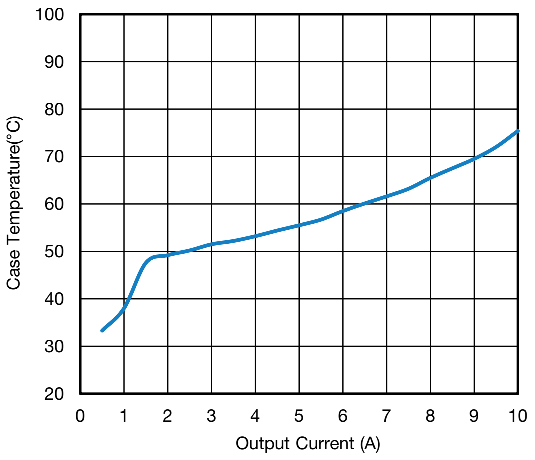

Fig. 13 - SiC461 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

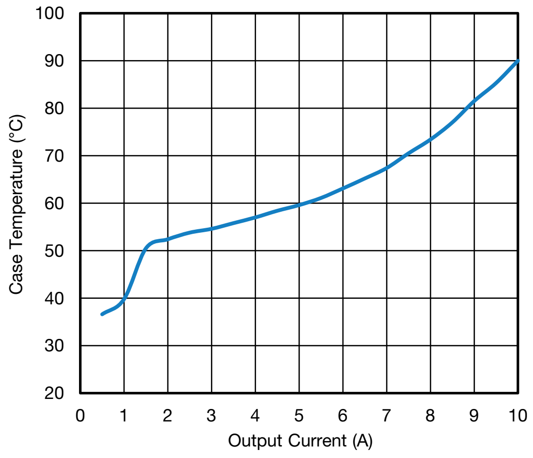

Fig. 16 - SiC461 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

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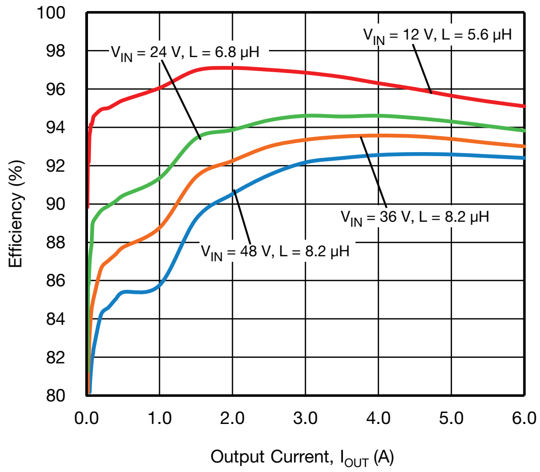

Fig. 17 - SiC462 Efficiency vs. Output Current, V_{OUT} = 5 V

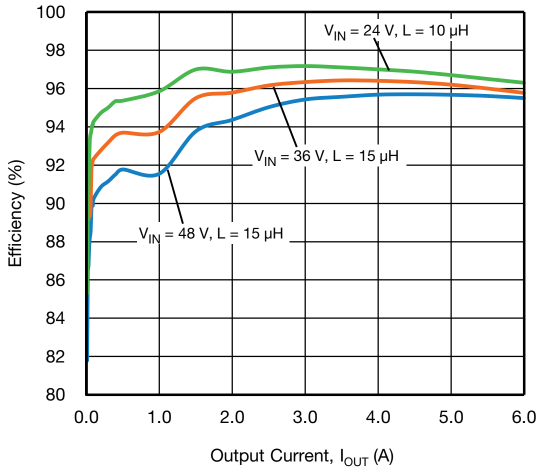

Fig. 18 - SiC462 Efficiency vs. Output Current, V_{OUT} = 12 V

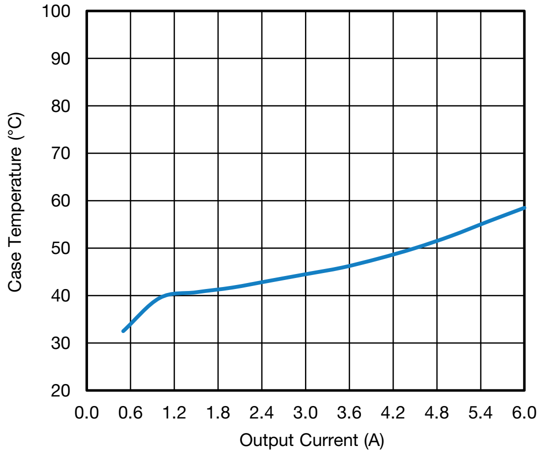

Fig. 19 - SiC462 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

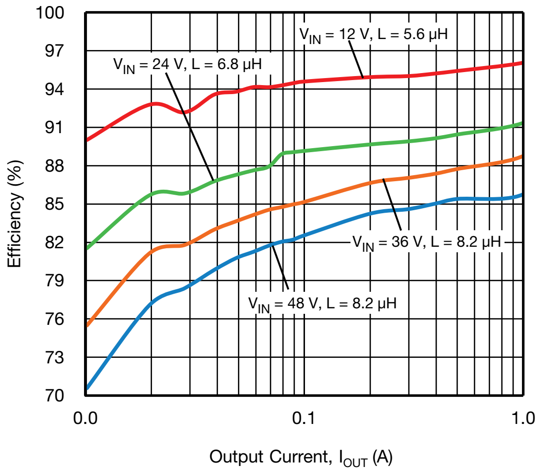

Fig. 20 - SiC462 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

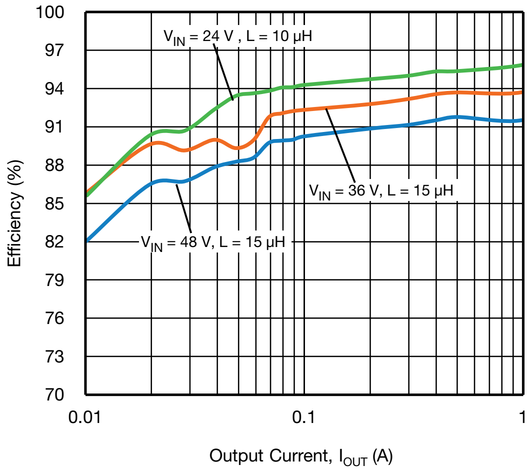

Fig. 21 - SiC462 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

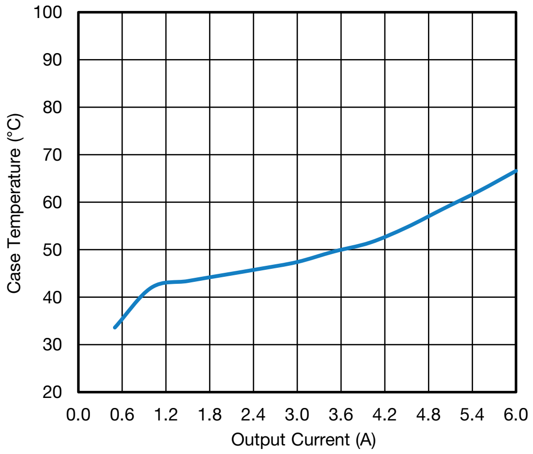

Fig. 22 - SiC462 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC463 (4 A), unless otherwise noted)

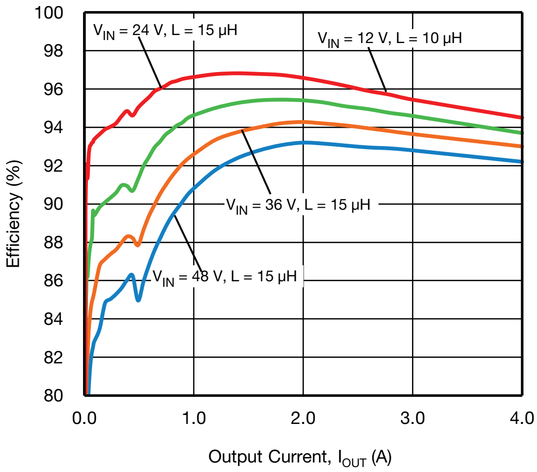

Fig. 23 - SiC463 Efficiency vs. Output Current, V_{OUT} = 5 V

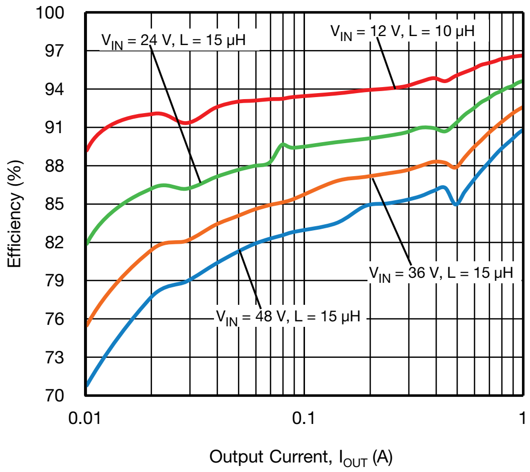

Fig. 26 - SiC463 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

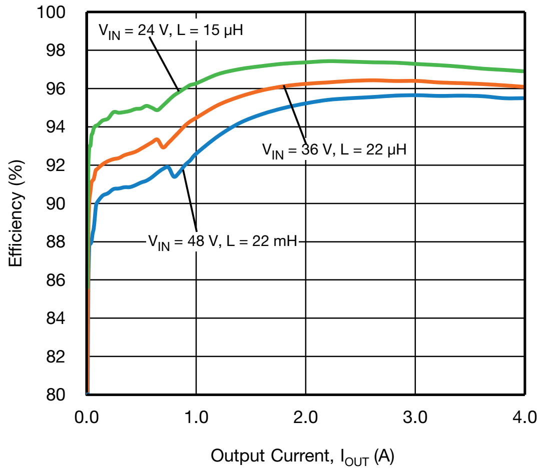

Fig. 24 - SiC463 Efficiency vs. Output Current, V_{OUT} = 12 V

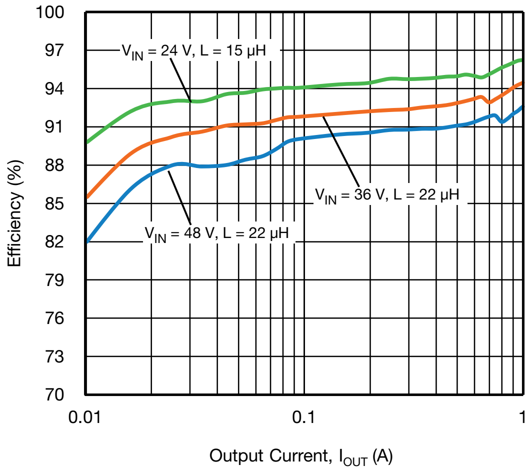

Fig. 27 - SiC463 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

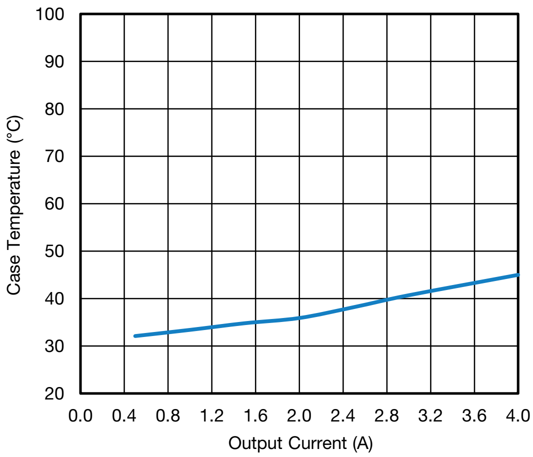

Fig. 25 - SiC463 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

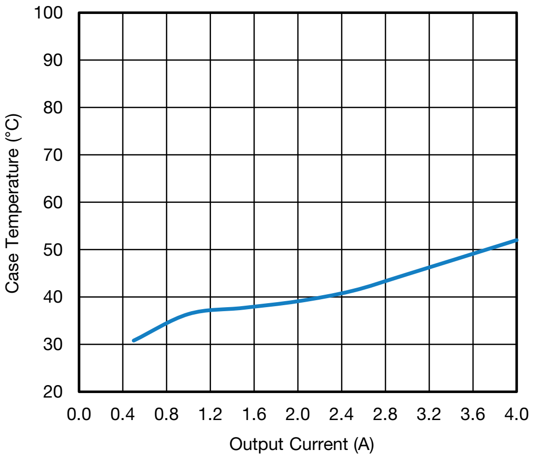

Fig. 28 - SiC463 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC464 (2 A), unless otherwise noted)

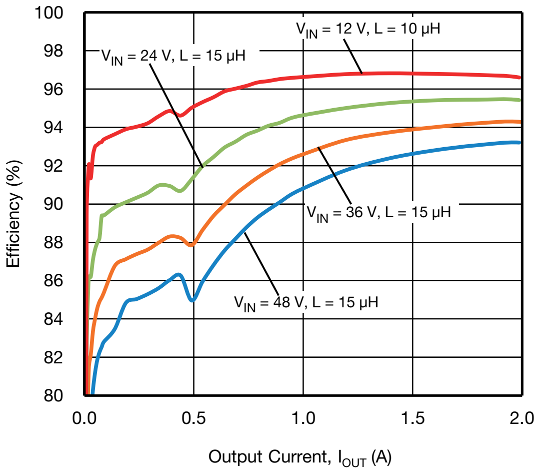

Fig. 29 - SiC464 Efficiency vs. Output Current, V_{OUT} = 5 V

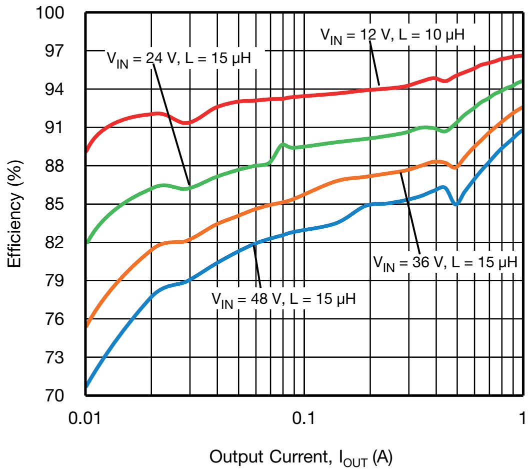

Fig. 32 - SiC464 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

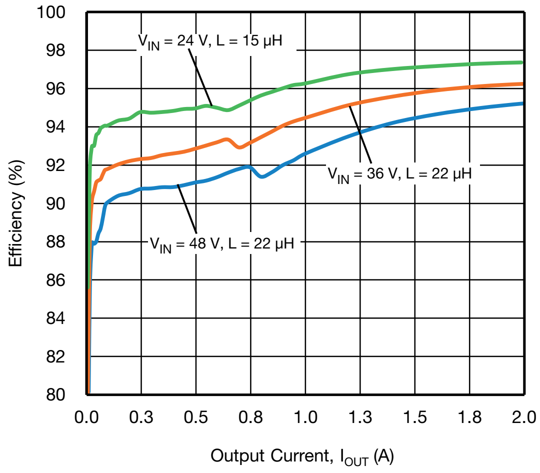

Fig. 30 - SiC464 Efficiency vs. Output Current, V_{OUT} = 12 V

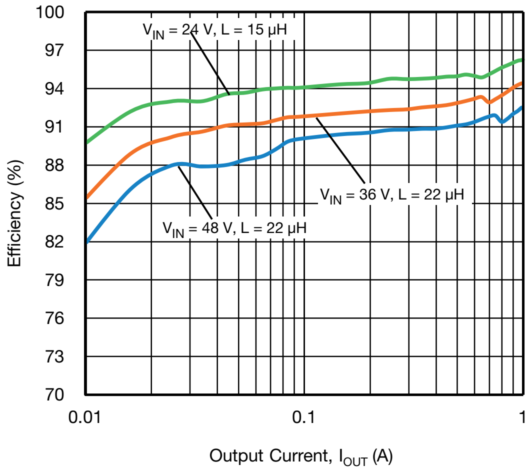

Fig. 33 - SiC464 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

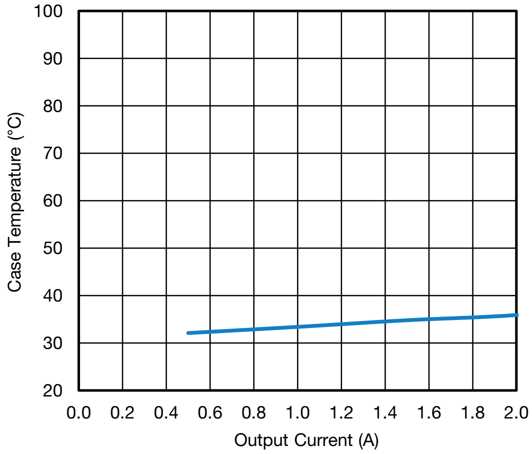

Fig. 31 - SiC464 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

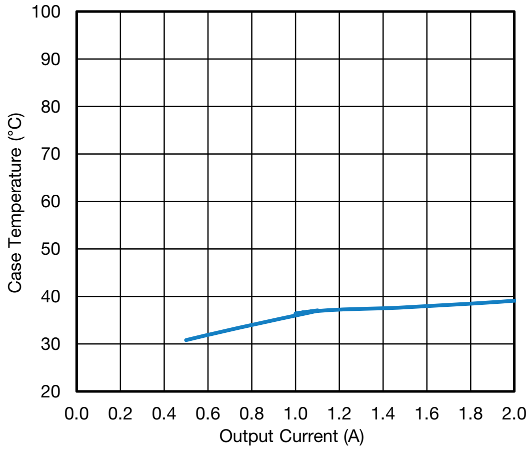

Fig. 34 - SiC464 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC462 (6 A), unless otherwise noted)

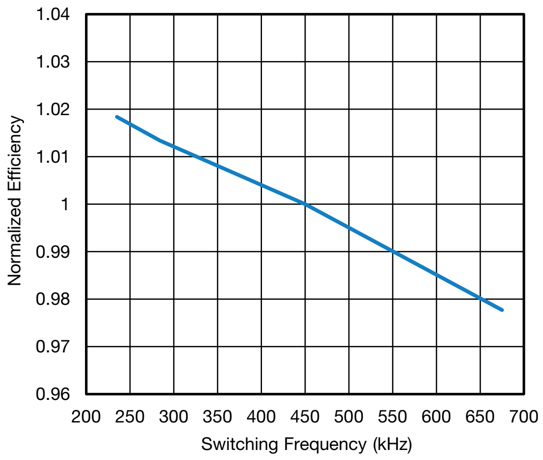

Fig. 35 - SiC461 Efficiency vs. Switching Frequency

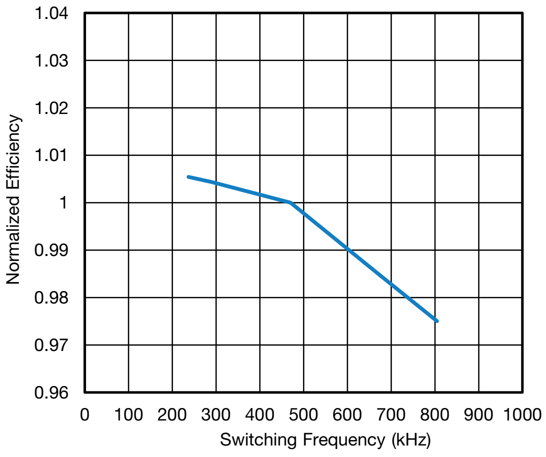

Fig. 38 - SiC462 Efficiency vs. Switching Frequency

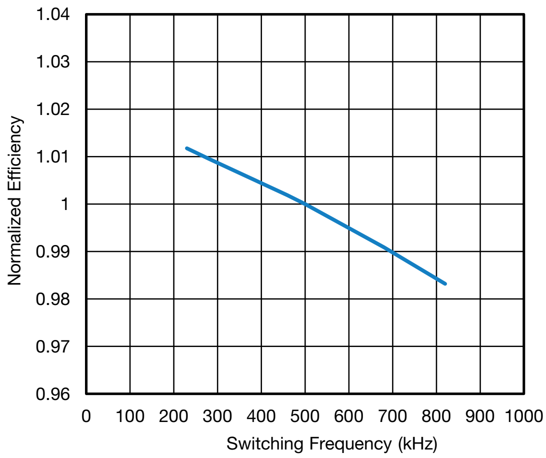

Fig. 36 - SiC463 Efficiency vs. Switching Frequency

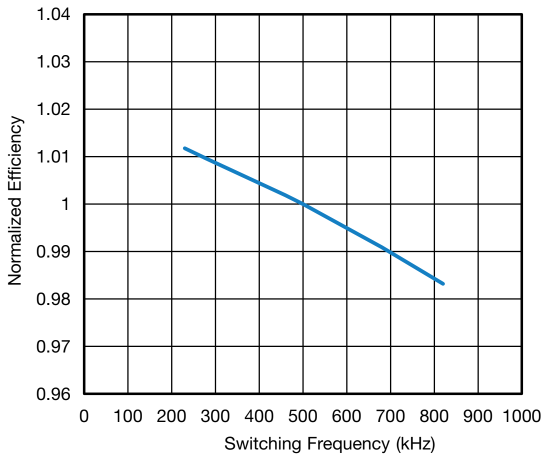

Fig. 39 - SiC464 Efficiency vs. Switching Frequency

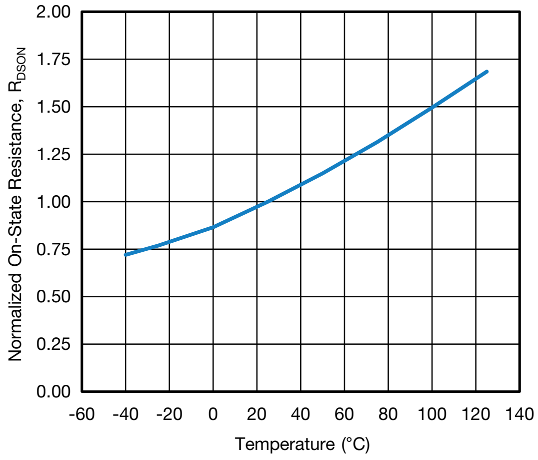

Fig. 37 - $R_{DS(ON)}$ vs. Temperature

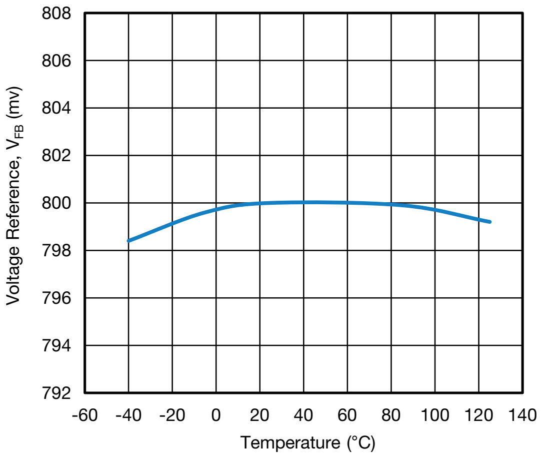

Fig. 40 - Voltage Reference vs. Temperature

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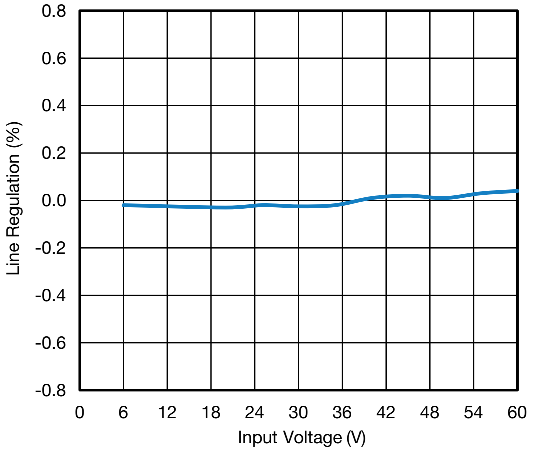

Fig. 41 - Line Regulation

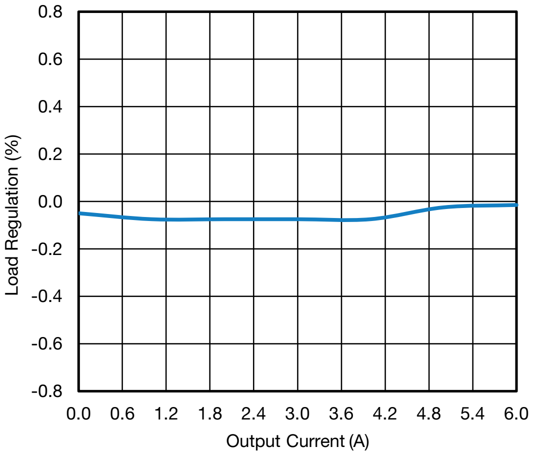

Fig. 44 - Load Regulation

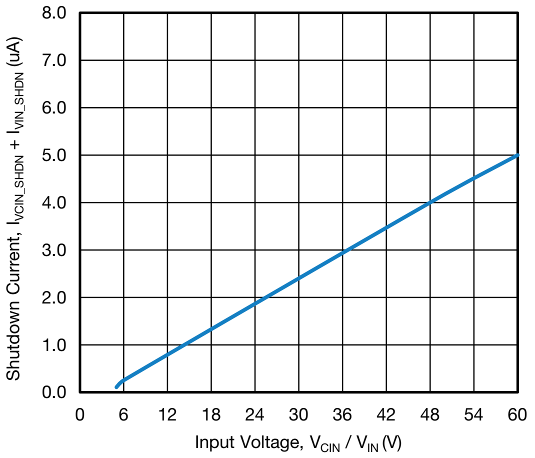

Fig. 42 - Shutdown Current vs. Input Voltage

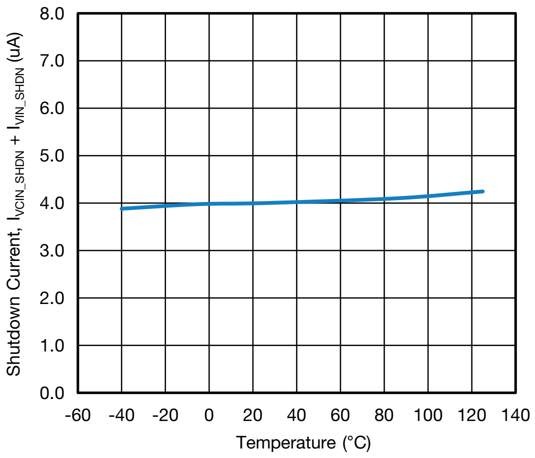

Fig. 45 - Shutdown Current vs. Junction Temperature

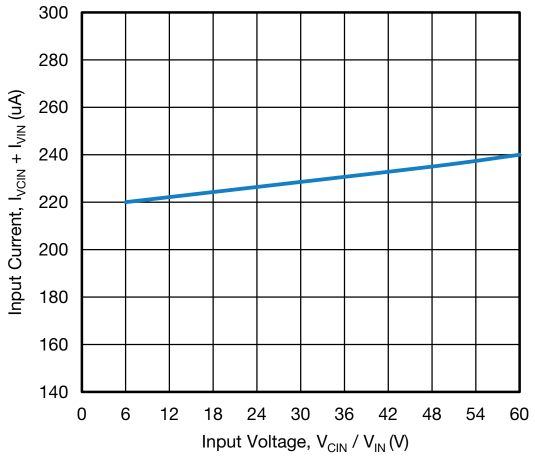

Fig. 43 - Input Current vs. Input Voltage

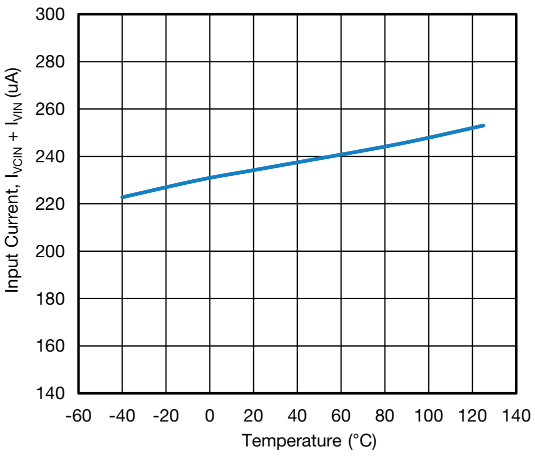

Fig. 46 - Input Current vs. Junction Temperature

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC462 (6 A), unless otherwise noted)

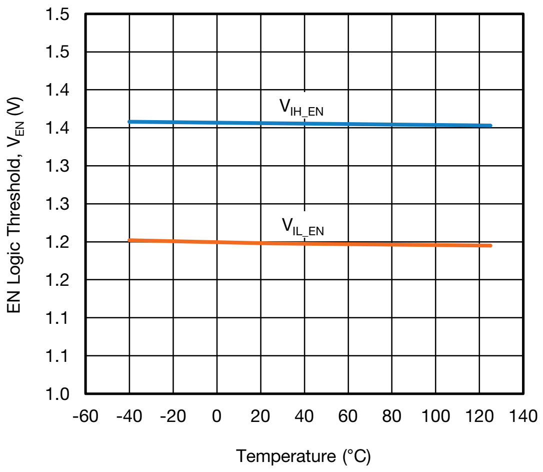

Fig. 47 - EN Logic Threshold vs. Junction Temperature

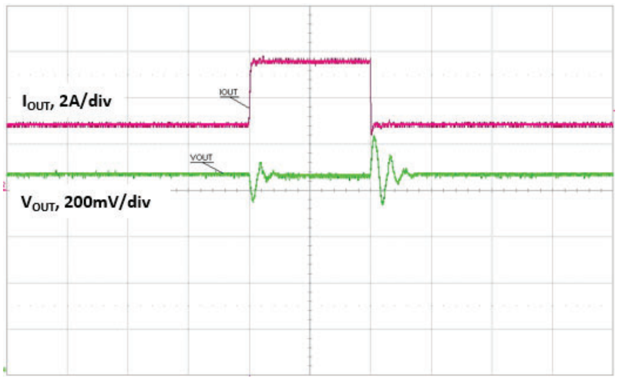

Fig. 48 - Load Transient (3 A to 6 A), Time = 100 µs/div

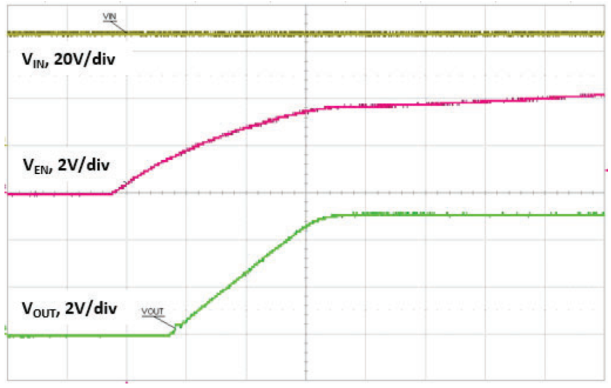

Fig. 49 - Start-Up with EN, Time = 1 ms/div

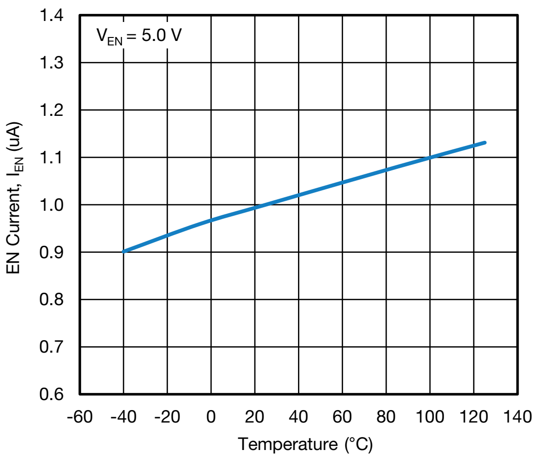

Fig. 50 - EN Current vs. Junction Temperature

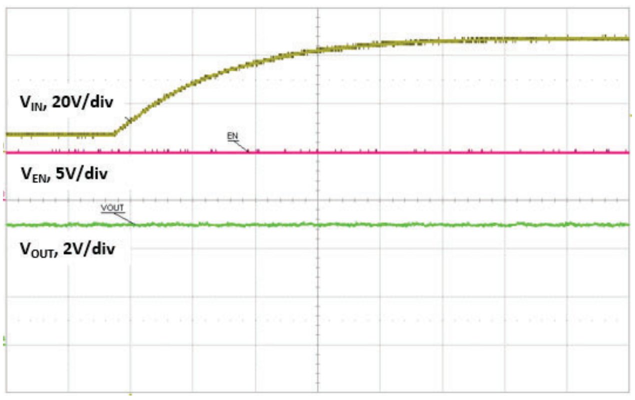

Fig. 51 - Line Transient (8 V to 48 V), Time = 10 ms/div

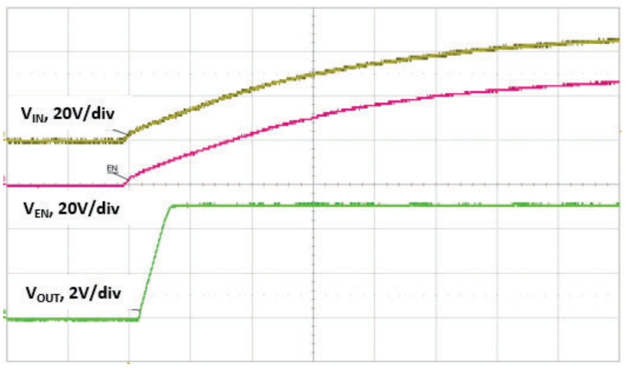

Fig. 52 - Start-up with V_{IN}, Time = 5 ms/div

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC462 (6 A), unless otherwise noted)

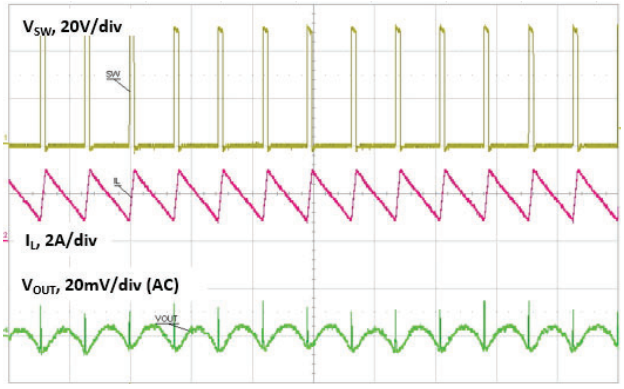

Fig. 53 - Output Ripple 2 A, Time = 5 μs/div

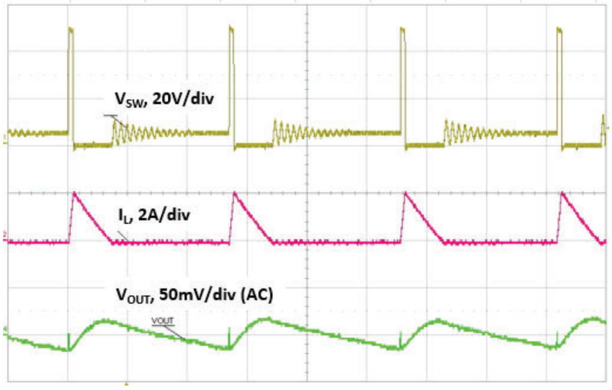

Fig. 55 - Output Ripple 300 mA, Time = 5 μs/div

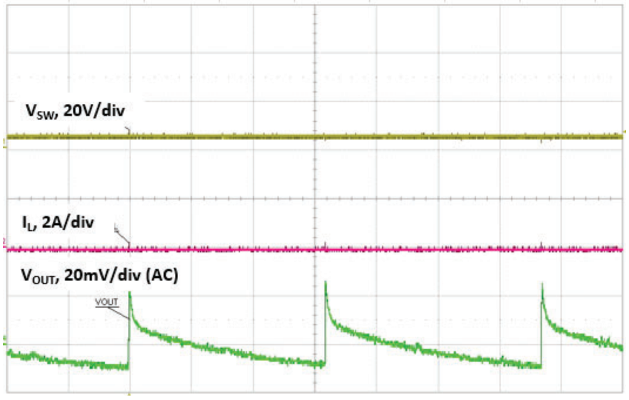

Fig. 54 - Output Ripple PSM, Time = 10 ms/div

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PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling

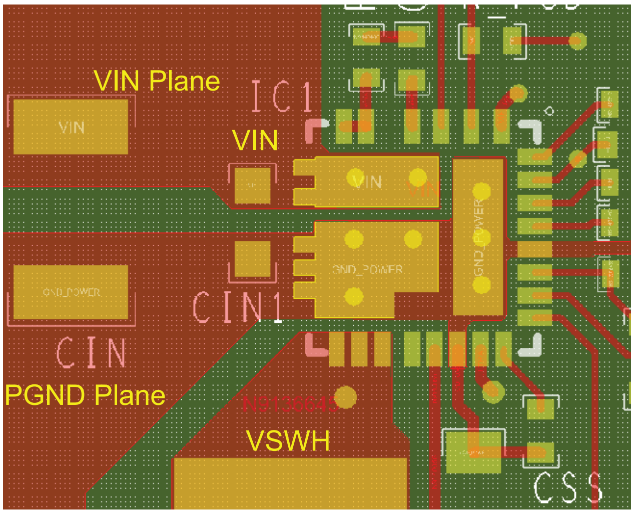

Fig. 56

5. Layout V_{IN} and P_{GND} planes as shown above
6. Ceramic capacitors should be placed between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
7. Various ceramic capacitor values and package sizes should be used to cover entire coupling spectrum e.g. 1210 and 0603
8. Smaller capacitance values, closer to V_{IN} pin(s), provide better high frequency response

Step 2: V_{CIN} Pin

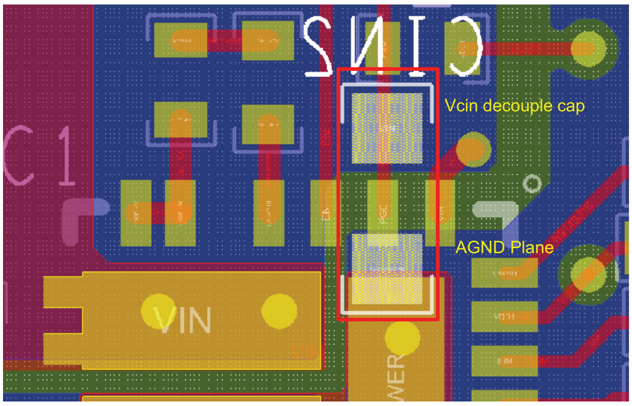

Fig. 57

1. V_{CIN} is the input pin for both internal LDO and t_{ON} block. t_{ON} varies with input voltage and it is necessary to put a decoupling capacitor close to this pin
2. The connection can be made through a via and the capacitor can be placed at bottom layer

Step 3: SW Plane

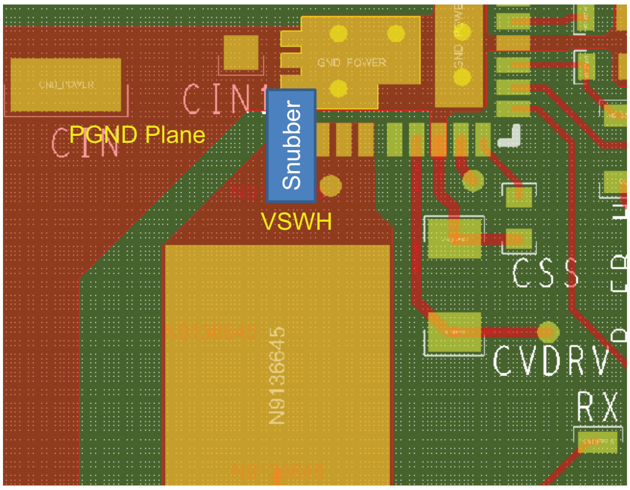

Fig. 58

1. Connect output inductor to device with large plane to lower resistance
2. If any snubber network is required, place the components on the bottom side as shown above

Step 4: V_{DD}/V_{DRV} Input Filter

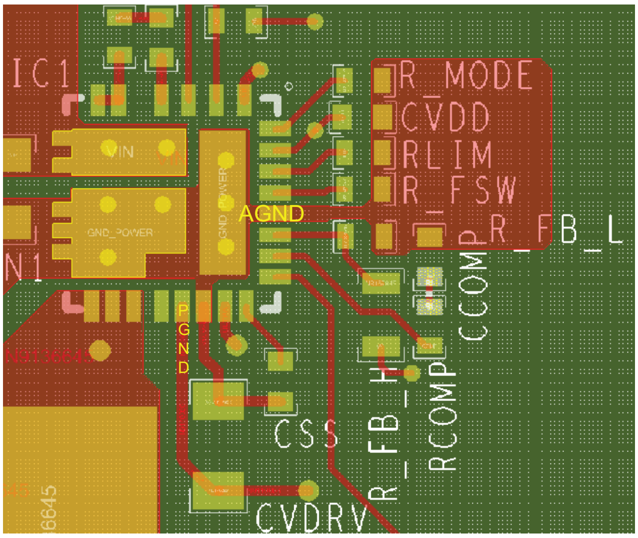

Fig. 59

1. C_{VDD} cap should be placed between V_{DD} and A_{GND} to achieve best noise filtering
2. C_{VDRV} cap should be placed close to V_{DRV} and P_{GND} pins to reduce effects of trace impedance and provide maximum instantaneous driver current for low side MOSFET during switching cycle

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Step 5: BOOT Resistor and Capacitor Placement

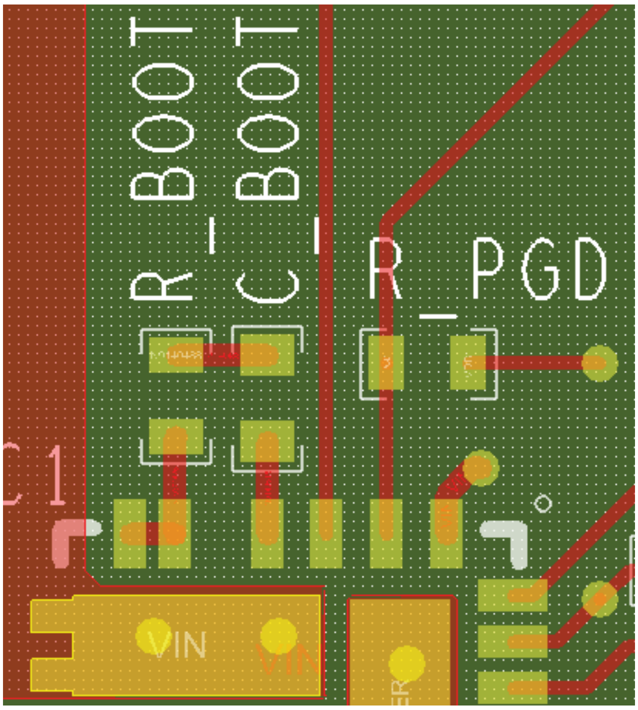

Fig. 60

1. C_{BOOT} and R_{BOOT} need to be placed very close to the device, between PHASE and BOOT pins
2. In order to reduce parasitic inductance, it is recommended to use 0402 chip size for the resistor and the capacitor

Step 6: Signal Routing

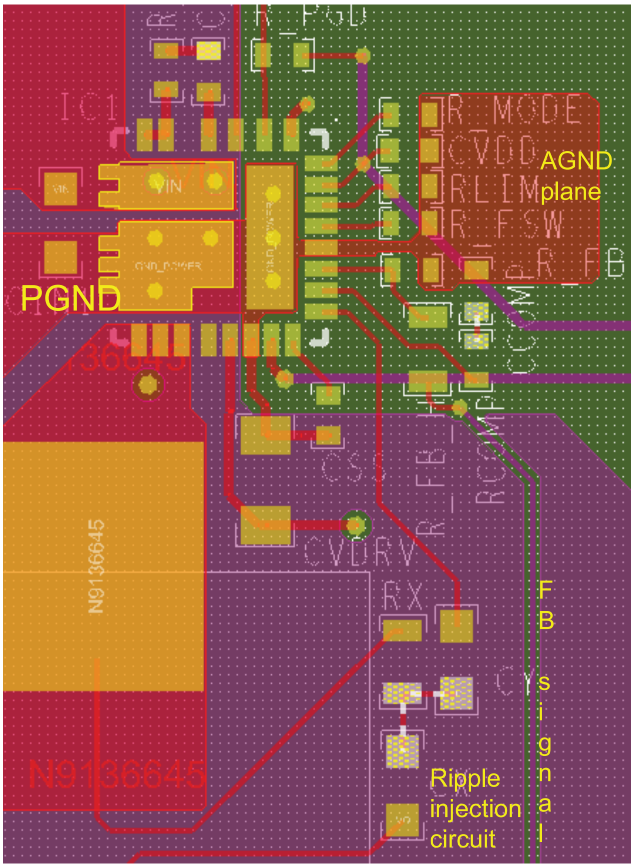

Fig. 61

1. Separate the small analog signal from high current path. As shown above, the high current paths with high dv/dt, di/dt are placed on the left side of the IC, while the small control signals are placed on the right side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length
2. IC analog ground (A_{GND}), pin 23, should have a single connection to P_{GND}. The A_{GND} ground plane connected to pin 23 helps to keep A_{GND} quiet and improves noise immunity
3. Feedback signal can be routed through inner layer. Make sure this signal is far from SW node and shielded by inner ground layer
4. Ripple injection circuit can be placed next to inductor. Kelvin connection as shown above is recommended

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Step 7: Adding Thermal Relief Vias and Duplicate Power Path Plane

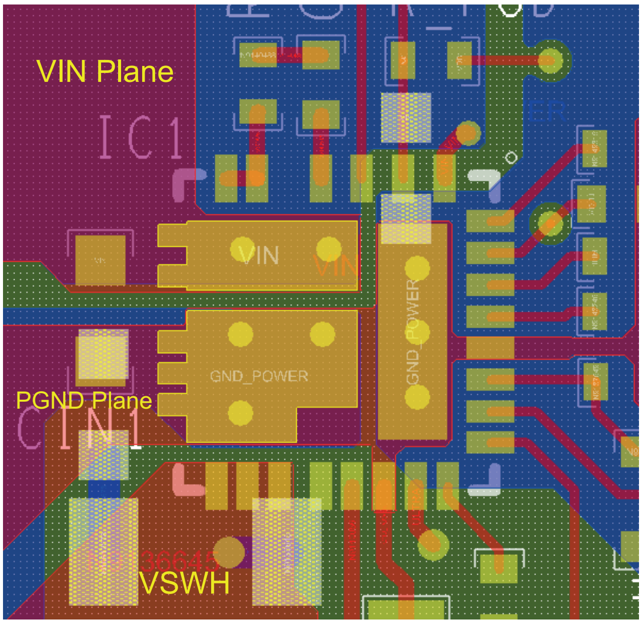

Fig. 62

1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional vias can be placed on V_{IN} and P_{GND} planes. It is also necessary to duplicate the V_{IN} and ground plane at bottom layer to maximize the power dissipation capability of the PCB
3. SW pad is a noise source and it is not recommended to place vias on this pad
4. 8 mil vias on pads and 10 mil vias on planes are ideal via sizes. The vias on pad may drain solder during assembly and cause assembly issues. Please consult with the assembly house for guideline

Step 8: Ground Layer

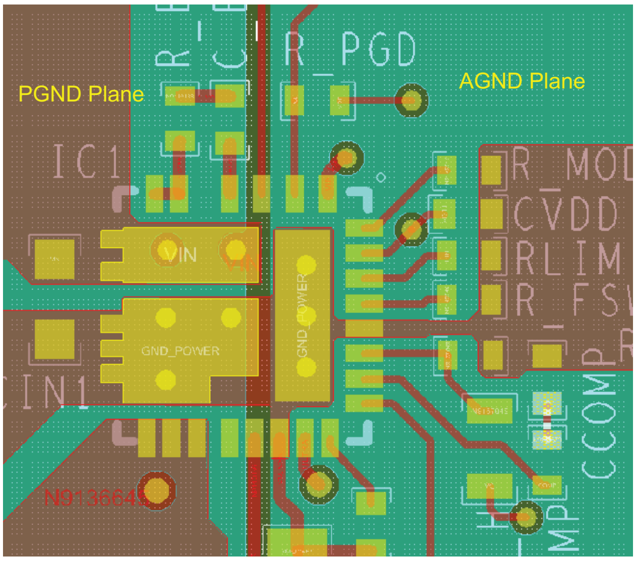

Fig. 63

1. It is recommended to make the entire inner layer (next to top layer) ground plane
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer
3. The ground plane can be broken into two sections, P_{GND} and A_{GND}

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PRODUCT SUMMARY				
Part number	SiC461	SiC462	SiC463	SiC464
Description	10 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous buck regulator	6 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous buck regulator	4 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous buck regulator	2 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous buck regulator
Input voltage min. (V)	4.5	4.5	4.5	4.5
Input voltage max. (V)	60	60	60	60
Output voltage min. (V)	0.8	0.8	0.8	0.8
Output voltage max. (V)	0.92 x V_{IN}	0.92 x V_{IN}	0.92 x V_{IN}	0.92 x V_{IN}
Continuous current (A)	10	6	4	2
Switch frequency min. (kHz)	100	100	100	100
Switch frequency max. (kHz)	2000	2000	2000	2000
Pre-bias operation (yes / no)	Yes	Yes	Yes	Yes
Internal bias reg. (yes / no)	Yes	Yes	Yes	Yes
Compensation	External	External	External	External
Enable (yes / no)	Yes	Yes	Yes	Yes
P_{GOOD} (yes / no)	Yes	Yes	Yes	Yes
Overcurrent protection	Yes	Yes	Yes	Yes
Protection	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO
Light load mode	Selectable powersave / ultrasonic	Selectable powersave / ultrasonic	Selectable powersave / ultrasonic	Selectable powersave / ultrasonic
Peak efficiency (%)	98	98	98	98
Package type	PowerPAK MLP55-27L	PowerPAK MLP55-27L	PowerPAK MLP55-27L	PowerPAK MLP55-27L
Package size (W, L, H) (mm)	5 x 5 x 0.75	5 x 5 x 0.75	5 x 5 x 0.75	5 x 5 x 0.75
Status code	2	2	2	2
Product type	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)
Applications	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking

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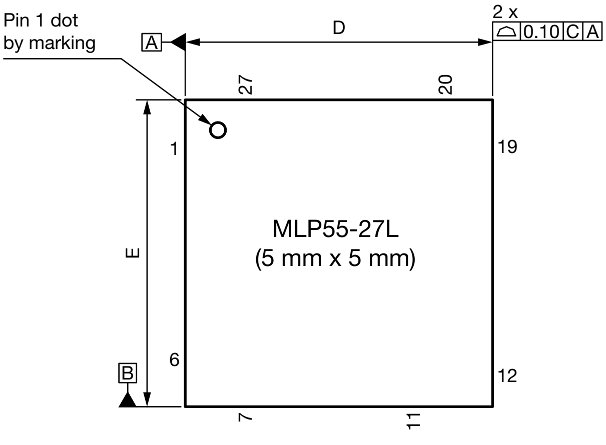
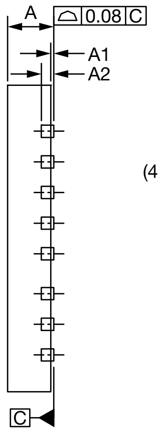
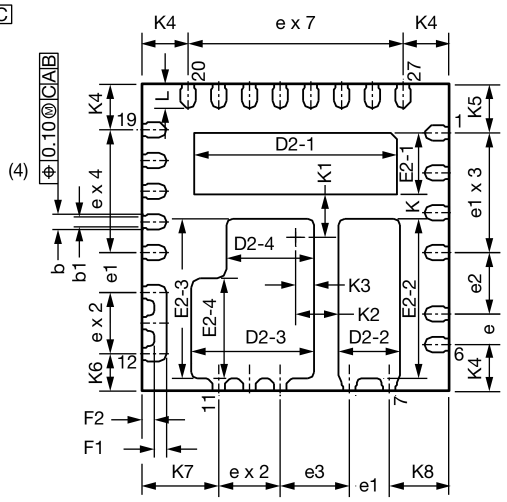
PowerPAK® MLP55-27 Case Outline



Top view



Side view



Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [8]	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b [4]	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.15	0.20	0.25	0.006	0.008	0.010
D	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.020 BSC		
e1	0.65 BSC			0.026 BSC		
e2	1.00 BSC			0.039 BSC		
e3	1.13 BSC			0.044 BSC		
E	5.00 BSC			0.197 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
N [3]	28			28		
D2-1	3.25	3.30	3.35	0.128	0.130	0.132
D2-2	0.95	1.00	1.05	0.037	0.039	0.041
D2-3	1.95	2.00	2.05	0.077	0.079	0.081
D2-4	1.37	1.42	1.47	0.054	0.056	0.058
E2-1	0.95	1.00	1.05	0.037	0.039	0.041
E2-2	2.55	2.60	2.65	0.100	0.102	0.104
E2-3	2.55	2.60	2.65	0.100	0.102	0.104
E2-4	1.58	1.63	1.68	0.062	0.064	0.066
F1	0.20	-	0.25	0.008	-	0.010
F2	min. 0.20			min. 0.008		

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DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
K	0.40 BSC			0.016 BSC		
K1	0.70 BSC			0.028 BSC		
K2	0.70 BSC			0.028 BSC		
K3	0.30 BSC			0.012 BSC		
K4	0.75 BSC			0.030 BSC		
K5	0.80 BSC			0.0315 BSC		
K6	0.60 BSC			0.024 BSC		
K7	1.25 BSC			0.049 BSC		
K8	0.975 BSC			0.038 BSC		
ECN: T18-0594-Rev. C, 03-Dec-2018 DWG: 6056						

Notes

(1) Use millimeters as the primary measurement

(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994

(3) N is the number of terminals
Nd is the number of terminals in x-direction
Ne is the number of terminals in y-direction

(4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip

(5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body

(6) Exact shape and size of this feature is optional

(7) Package warpage max. 0.08 mm

(8) Applied only for terminals

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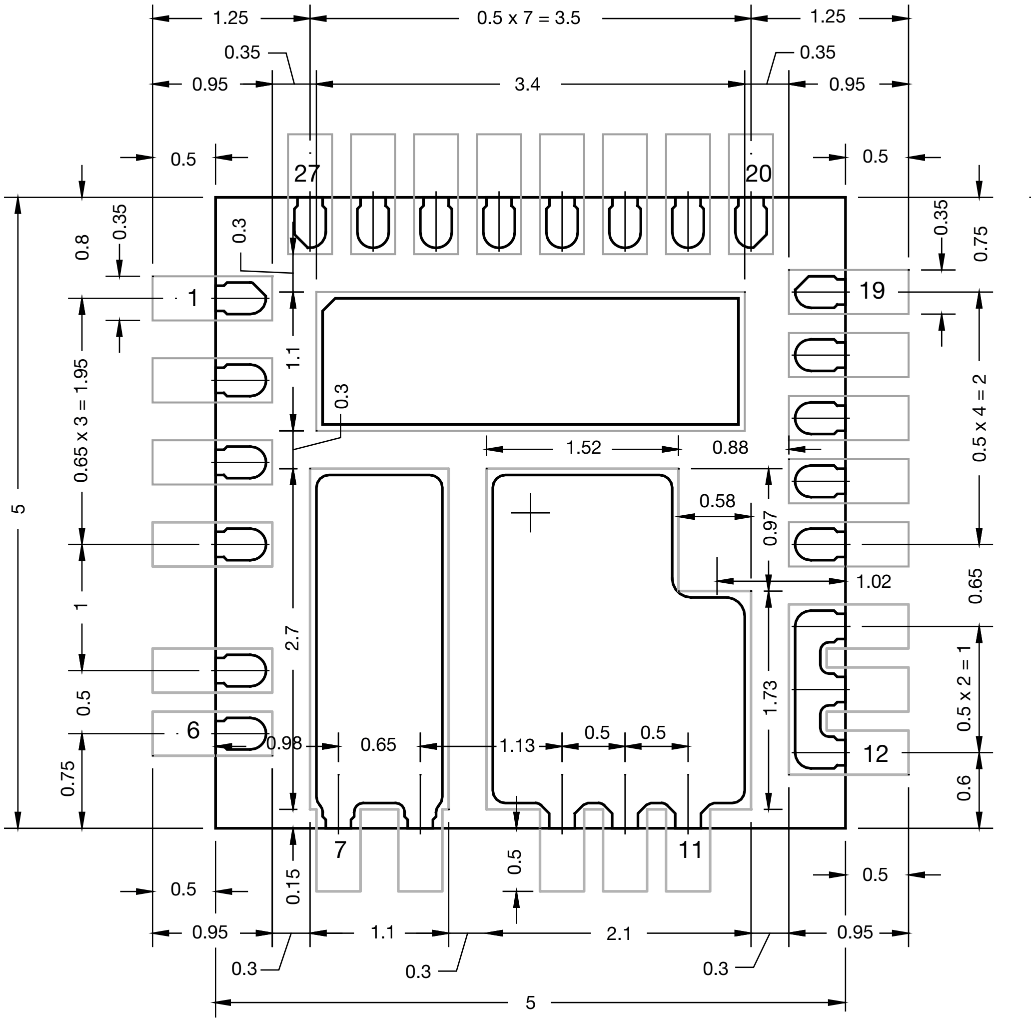
Recommended Land Pattern
PowerPAK® MLP55-27L



All dimensions in millimeters

■ Component for MLP55-27L

☐ Land pattern for MLP55-27L

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