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VND5T016ASPTR-E

STMicroelectronics

Gate Drivers Double CH High-Side 41V 16mOhm 70A

Any questions, please feel free to contact us.
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Double channel high side driver with analog CurrentSense for 24 V automotive applications

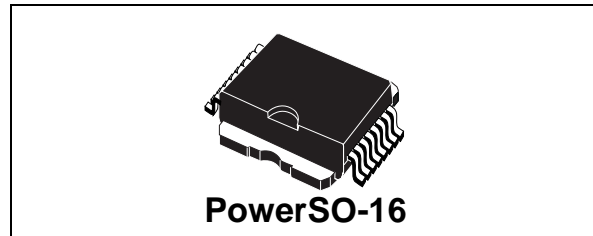
Datasheet – production data

Features

| | | |
|-----------------------------------|-----------|--------------------------|
| Max transient supply voltage | V_{CC} | 58 V |
| Operating voltage range | V_{CC} | 8 to 36 V |
| Typ ON-state resistance (per ch.) | R_{ON} | 16 m Ω |
| Current limitation (typ) | I_{LIM} | 70 A |
| OFF-state supply current | I_S | 2 μ A ⁽¹⁾ |

1. Typical value with all loads connected.

- General
 - Very low standby current
 - 3.0 V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - Compliance with European directive 2002/95/EC
 - Fault reset standby pin (FR_Stby)
- Diagnostic functions
 - Proportional load current sense
 - Current sense precision for wide range currents
 - Off state open load detection
 - Output short to V_{CC} detection
 - Overload and short to ground latch-off
 - Thermal shutdown latch-off
 - Very low current sense leakage
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}
 - Thermal shutdown
 - Reverse battery protected with self switch of the PowerMOS
 - Electrostatic discharge protection



Application

- All types of resistive, inductive and capacitive loads

Description

The VND5T016ASP-E is a device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes. This device integrates an analog current sense which delivers a current proportional to the load current. Fault conditions such as overload, overtemperature or short to V_{CC} are reported via the current sense pin.

Output current limitation protects the device in overload condition. The device will latch off in case of overload or thermal shutdown.

The device is reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and fault reset standby pin disables all outputs and sets the device in standby mode.

Contents

- 1 Block diagram and pin description 5**
- 2 Electrical specifications 7**
 - 2.1 Absolute maximum ratings 7
 - 2.2 Thermal data 8
 - 2.3 Electrical characteristics 9
 - 2.4 Electrical characteristics curves 19
 - 2.5 Maximum demagnetization energy ($V_{CC} = 24\text{ V}$) 21
- 3 Package and PCB thermal data 22**
 - 3.1 PowerSO-16 thermal data 22
- 4 Package information 25**
 - 4.1 ECOPACK[®] 25
 - 4.2 PowerSO-16 mechanical data 25
 - 4.3 Packing information 27
- 5 Order codes 29**
- 6 Revision history 30**

List of tables

| | | |
|-----------|---|----|
| Table 1. | Pin function | 5 |
| Table 2. | Suggested connections for unused and not connected pins | 6 |
| Table 3. | Absolute maximum ratings | 7 |
| Table 4. | Thermal data | 8 |
| Table 5. | Power section | 9 |
| Table 6. | Switching ($V_{CC} = 24V$; $T_j = 25^{\circ}C$) | 9 |
| Table 7. | Logic inputs. | 10 |
| Table 8. | Protections and diagnostics | 11 |
| Table 9. | Current sense ($8 V < V_{CC} < 36 V$) | 12 |
| Table 10. | Openload detection ($FR_Stby = 5 V$) | 13 |
| Table 11. | Truth table. | 17 |
| Table 12. | Electrical transient requirements (part 1) | 18 |
| Table 13. | Electrical transient requirements (part 2) | 18 |
| Table 14. | Electrical transient requirements (part 3) | 18 |
| Table 15. | Thermal parameters | 24 |
| Table 16. | PowerSO-16 mechanical data | 26 |
| Table 17. | Device summary | 29 |
| Table 18. | Document revision history | 30 |

List of figures

| | | |
|------------|--|----|
| Figure 1. | Block diagram | 5 |
| Figure 2. | Configuration diagram (top view) | 6 |
| Figure 3. | Current and voltage conventions | 7 |
| Figure 4. | t_{reset} definition | 10 |
| Figure 5. | t_{stby} definition | 11 |
| Figure 6. | Output stuck to V_{CC} detection delay time at FR_Stby activation | 14 |
| Figure 7. | Current sense delay characteristics | 14 |
| Figure 8. | Open-load off-state delay timing | 14 |
| Figure 9. | Switching characteristics | 15 |
| Figure 10. | Delay response time between rising edge of output current and rising edge of current sense | 16 |
| Figure 11. | Output voltage drop limitation | 16 |
| Figure 12. | Device behavior in overload condition | 17 |
| Figure 13. | Off-state output current | 19 |
| Figure 14. | High level input current | 19 |
| Figure 15. | Input clamp voltage | 19 |
| Figure 16. | Input low level voltage | 19 |
| Figure 17. | Input high level voltage | 19 |
| Figure 18. | Input hysteresis voltage | 19 |
| Figure 19. | On-state resistance vs T_{case} | 20 |
| Figure 20. | On-state resistance vs V_{CC} | 20 |
| Figure 21. | I_{LIMH} vs T_{case} | 20 |
| Figure 22. | Turn-on voltage slope | 20 |
| Figure 23. | Turn-off voltage slope | 20 |
| Figure 24. | Maximum turn-off current versus inductance | 21 |
| Figure 25. | PowerSO-16 PC board | 22 |
| Figure 26. | $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON) | 22 |
| Figure 27. | PowerSO-16 thermal impedance junction ambient single pulse (one channel ON) | 23 |
| Figure 28. | Thermal fitting model of a double channel HSD in PowerSO-16 | 23 |
| Figure 29. | PowerSO-16 package dimensions | 25 |
| Figure 30. | PowerSO-16 tube shipment (no suffix) | 27 |
| Figure 31. | PowerSO-16 tape and reel shipment (suffix "TR") | 27 |
| Figure 32. | PowerSO-16 suggested pad layout | 28 |

1 Block diagram and pin description

Figure 1. Block diagram

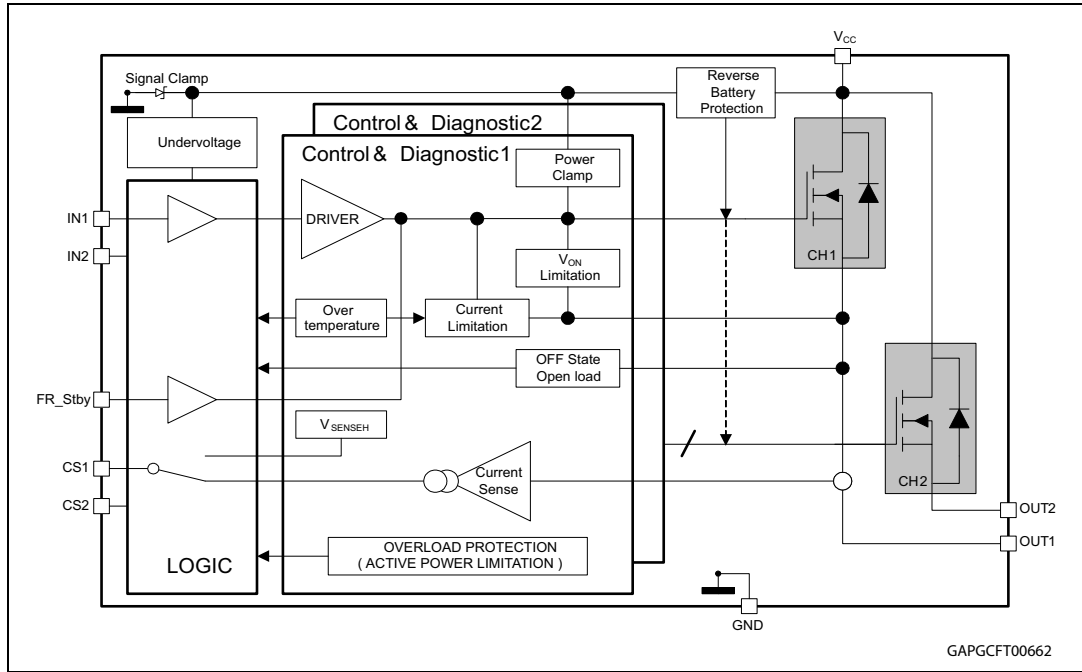


Table 1. Pin function

| Name | Function |
|-----------------|--|
| V _{CC} | Battery connection |
| OUTn | Power output |
| GND | Ground connection |
| INn | Voltage controlled input pin with hysteresis, CMOS-compatible; they control output switch state |
| CSn | Analog current sense pin, they deliver a current proportional to the load current |
| FR_Stby | In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low. |

Figure 2. Configuration diagram (top view)

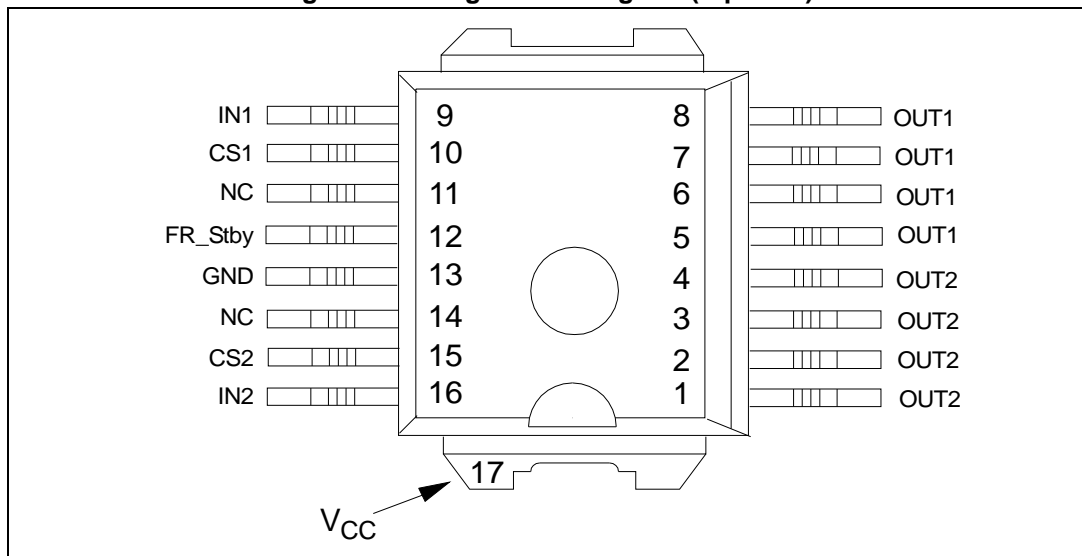


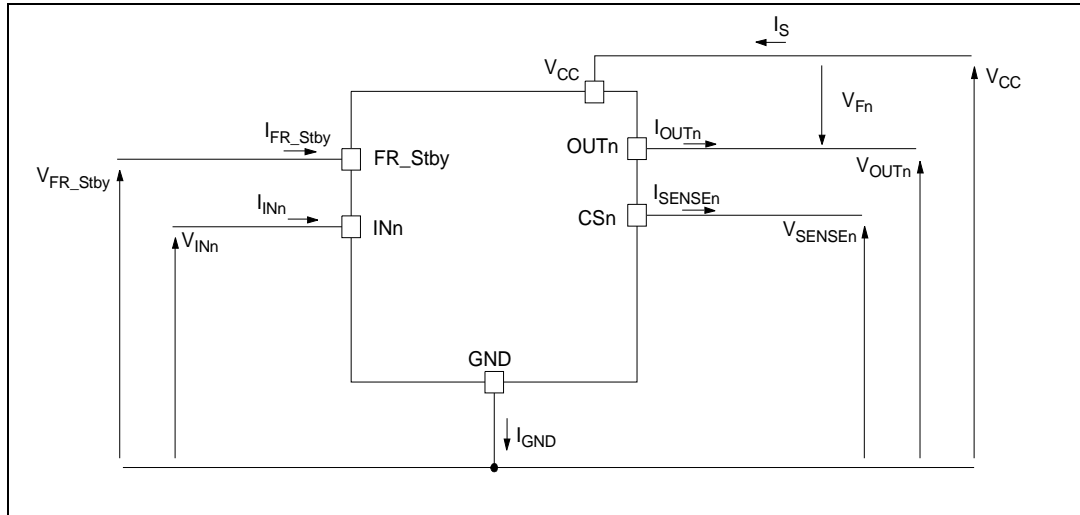
Table 2. Suggested connections for unused and not connected pins

| Connection / pin | Current Sense | N.C. | Output | Input | FR_Stby |
|------------------|------------------------|------------------|-------------|------------------------|------------------------|
| Floating | Not allowed | X ⁽¹⁾ | X | X | X |
| To ground | Through 10 kΩ resistor | X | Not allowed | Through 10 kΩ resistor | Through 10 kΩ resistor |

1. X: do not care.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--|--------------------------|---------------|
| V_{CC} | DC supply voltage | 58 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 32 | V |
| I_{OUT} | DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 45 | A |
| I_{IN} | DC input current | -1 to 10 | mA |
| I_{FR_Stby} | Fault reset standby DC input current | -1 to 1.5 | mA |
| $V_{CSSENSE}$ | Current sense maximum voltage | $V_{CC}-58$ to $+V_{CC}$ | V |
| E_{MAX} | Maximum switching energy ($L = 11$ mH; $V_{bat} = 32$ V; $T_{jstart} = 150^{\circ}\text{C}$; $I_{OUT} = 5.3$ A) | 320 | mJ |
| L_{SMAX} | Maximum stray inductance in short circuit condition $R_L = 300$ m Ω ; $V_{BAT} = 32$ V; $T_{jstart} = 150^{\circ}\text{C}$; $I_{OUT} = I_{limH_max}$ | 40 | μH |

Table 3. Absolute maximum ratings (continued)

| Symbol | Parameter | Value | Unit |
|------------------|---|------------|------|
| V _{ESD} | Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) | | |
| | – INPUT | 4000 | V |
| | – CURRENT SENSE | 2000 | V |
| | – FAULT RESET STANDBY PIN | 4000 | V |
| | – OUTPUT | 5000 | V |
| | – V _{CC} | 5000 | V |
| V _{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| T _j | Junction operating temperature | -40 to 150 | °C |
| T _{stg} | Storage temperature | -55 to 150 | °C |

2.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|---|-------------------------------|------|
| R _{thj-case} | Thermal resistance junction-case (Max.) (with one channel ON) | 0.9 | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient (Max.) | See Figure 26 | °C/W |

2.3 Electrical characteristics

$8\text{ V} < V_{CC} < 36\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified.

Table 5. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------------|---|------|------------------|------|------|
| V_{CC} | Operating supply voltage | | 8 | 24 | 36 | V |
| V_{USD} | Undervoltage shutdown | | | 3.5 | 5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.5 | | V |
| R_{ON} | On state resistance ⁽¹⁾ | $I_{OUT} = 5\text{ A}$; $T_j = 25^{\circ}\text{C}$; $8\text{ V} < V_{CC} < 36\text{ V}$ | | 16 | | mΩ |
| | | $I_{OUT} = 5\text{ A}$; $T_j = 150^{\circ}\text{C}$; $8\text{ V} < V_{CC} < 36\text{ V}$ | | | 32 | |
| $R_{ON REV}$ | Reverse battery ON state resistance | $V_{CC} = -24\text{ V}$; $I_{OUT} = -5\text{ A}$; $T_j = 25^{\circ}\text{C}$ | | | 16 | mΩ |
| V_{clamp} | Clamp voltage | $I_S = 20\text{ mA}$ | 58 | 64 | 70 | V |
| I_S | Supply current | Off-state; $V_{CC} = 24\text{ V}$; $T_j = 25^{\circ}\text{C}$; $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$ | | 2 ⁽²⁾ | 5 | μA |
| | | On-state; $V_{CC} = 24\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$ | | 4.5 | 6.5 | mA |
| $I_{L(off1)}$ | Off state output current | $V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $T_j = 25^{\circ}\text{C}$ | 0 | 0.01 | 3 | μA |
| | | $V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $T_j = 125^{\circ}\text{C}$ | 0 | | 5 | |

1. For each channel
2. PowerMOS leakage included.

Table 6. Switching ($V_{CC} = 24\text{V}$; $T_j = 25^{\circ}\text{C}$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|---------------------|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $R_L = 4.8\ \Omega$ | — | 50 | — | μs |
| $t_{d(off)}$ | Turn-off delay time | $R_L = 4.8\ \Omega$ | — | 45 | — | μs |
| $dV_{OUT}/dt_{(on)}$ | Turn-on voltage slope | $R_L = 4.8\ \Omega$ | | 0.65 | | V/μs |
| $dV_{OUT}/dt_{(off)}$ | Turn-off voltage slope | $R_L = 4.8\ \Omega$ | | 0.6 | | V/μs |
| W_{ON} | Switching energy losses during t_{won} | $R_L = 4.8\ \Omega$ | — | 2.1 | — | mJ |
| W_{OFF} | Switching energy losses during t_{woff} | $R_L = 4.8\ \Omega$ | — | 0.9 | — | mJ |

Table 7. Logic inputs

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|--|---------------------------------------|------|------|------|---------------|
| V_{IL} | Input low level voltage | | | | 0.9 | V |
| I_{IL} | Low level input current | $V_{IN} = 0.9\text{ V}$ | 1 | | | μA |
| V_{IH} | Input high level voltage | | 2.1 | | | V |
| I_{IH} | High level input current | $V_{IN} = 2.1\text{ V}$ | | | 10 | μA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.25 | | | V |
| V_{ICL} | Input clamp voltage | $I_{IN} = 1\text{ mA}$ | 5.5 | | 7 | V |
| | | $I_{IN} = -1\text{ mA}$ | | -0.7 | | |
| $V_{FR_Stby_L}$ | Fault_reset_standby low level voltage | | | | 0.9 | V |
| $I_{FR_Stby_L}$ | Low level fault_reset_standby current | $V_{FR_Stby} = 0.9\text{ V}$ | 1 | | | μA |
| $V_{FR_Stby_H}$ | Fault_reset_standby high level voltage | | 2.1 | | | V |
| $I_{FR_Stby_H}$ | High level fault_reset_standby current | $V_{FR_Stby} = 2.1\text{ V}$ | | | 10 | μA |
| $V_{FR_Stby(hyst)}$ | Fault_reset_standby hysteresis voltage | | 0.25 | | | V |
| $V_{FR_Stby_CL}$ | Fault_reset_standby clamp voltage | $I_{FR_Stby} = 15\text{ mA (10 ms)}$ | 11 | | 15 | V |
| | | $I_{FR_Stby} = -1\text{ mA}$ | | -0.7 | | |
| t_{reset} | Overload latch-off reset time | See Figure 5 | 2 | | 24 | μs |
| t_{stby} | Standby delay | See Figure 4 | 120 | | 1200 | μs |

Figure 4. t_{reset} definition

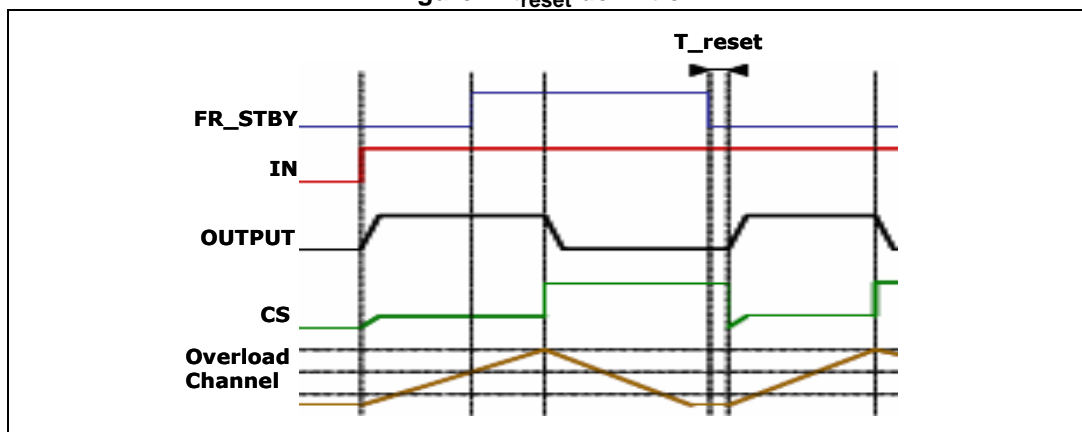


Figure 5. t_{stby} definition

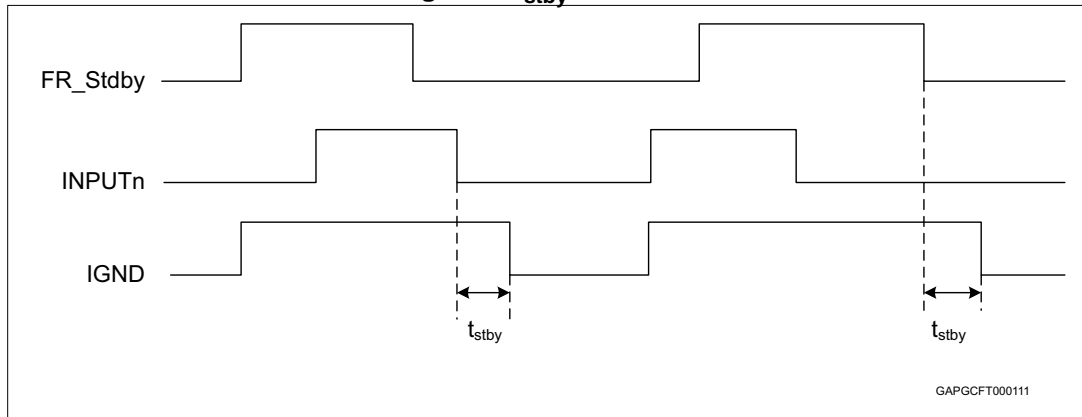


Table 8. Protections and diagnostics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|--|--|---------------|---------------|---------------|------|
| I_{limH} | DC short circuit current | $V_{CC} = 24\text{ V}$ | 45 | 70 | 90 | A |
| | | $5\text{ V} < V_{CC} < 36\text{ V}$ | | | 90 | A |
| I_{limL} | Short circuit current during thermal cycling | $V_{CC} = 24\text{ V};$ $T_R < T_j < T_{TSD}$ | | 16 | | A |
| T_{TSD} | Shutdown temperature | | 150 | 175 | 200 | °C |
| T_R | Reset temperature | | $T_{RS} + 1$ | $T_{RS} + 5$ | | °C |
| T_{RS} | Thermal reset of status | | 135 | | | °C |
| T_{HYST} | Thermal hysteresis ($T_{TSD} - T_R$) | | | 7 | | °C |
| V_{DEMAG} | Turn-off output voltage clamp | $I_{OUT} = 5\text{ A}; V_{IN} = 0;$ $L = 6\text{ mH}$ | $V_{CC} - 58$ | $V_{CC} - 64$ | $V_{CC} - 70$ | V |
| V_{ON} | Output voltage drop limitation | $I_{OUT} = 500\text{ mA}$ | | 25 | | mV |

Table 9. Current sense (8 V < V_{CC} < 36 V)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------------------|------------------------------|--|--------------|------|--------------|---------------|
| $dK_{I_{LED}}/K_{I_{LED}(TOT)}^{(1)}$ | Current sense ratio drift | $I_{OUT} = 12 \text{ mA to } 100 \text{ mA};$ $I_{CAL} = 50 \text{ mA}; V_{SENSE} = 0.5 \text{ V}$ | -50 | | 50 | % |
| K_0 | I_{OUT}/I_{SENSE} | $I_{OUT} = 100 \text{ mA}; V_{SENSE} = 0.5 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | 1185 | 5770 | 10760 | |
| $dK_0/K_0^{(1)}$ | Current sense ratio drift | $I_{OUT} = 100 \text{ mA}; V_{SENSE} = 0.5 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | -25 | | 25 | % |
| K_1 | I_{OUT}/I_{SENSE} | $I_{OUT} = 0.6 \text{ A}; V_{SENSE} = 1 \text{ V};$ $T_j = -40^\circ\text{C...}150^\circ\text{C}$ $T_j = 25^\circ\text{C...}150^\circ\text{C}$ | 2225 3000 | 5350 | 8580 7500 | |
| $dK_1/K_1^{(1)}$ | Current sense ratio drift | $I_{OUT} = 0.6 \text{ A}; V_{SENSE} = 1 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | -20 | | 20 | % |
| K_2 | I_{OUT}/I_{SENSE} | $I_{OUT} = 1.6 \text{ A}; V_{SENSE} = 1 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ $T_j = 25^\circ\text{C to } 150^\circ\text{C}$ | 2935 3250 | 4650 | 7305 6200 | |
| $dK_2/K_2^{(1)}$ | Current sense ratio drift | $I_{OUT} = 1.6 \text{ A}; V_{SENSE} = 1 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | -22 | | 17 | % |
| K_3 | I_{OUT}/I_{SENSE} | $I_{OUT} = 2.4 \text{ A}; V_{SENSE} = 2 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ $T_j = 25^\circ\text{C to } 150^\circ\text{C}$ | 2800 2955 | 4200 | 6680 5560 | |
| $dK_3/K_3^{(1)}$ | Current sense ratio drift | $I_{OUT} = 2.4 \text{ A}; V_{SENSE} = 2 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | -16 | | 23 | % |
| K_4 | I_{OUT}/I_{SENSE} | $I_{OUT} = 3 \text{ A}; V_{SENSE} = 4 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ $T_j = 25^\circ\text{C to } 150^\circ\text{C}$ | 2850 3170 | 4200 | 6000 5270 | |
| $dK_4/K_4^{(1)}$ | Current sense ratio drift | $I_{OUT} = 3 \text{ A}; V_{SENSE} = 4 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | -17 | | 17 | % |
| K_5 | I_{OUT}/I_{SENSE} | $I_{OUT} = 4.2 \text{ A}; V_{SENSE} = 4 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ $T_j = 25^\circ\text{C to } 150^\circ\text{C}$ | 3200 3450 | 4200 | 5400 4965 | |
| $dK_5/K_5^{(1)}$ | Current sense ratio drift | $I_{OUT} = 4.2 \text{ A}; V_{SENSE} = 4 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | -13 | | 13 | % |
| K_6 | I_{OUT}/I_{SENSE} | $I_{OUT} = 20 \text{ A}; V_{SENSE} = 4 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | 3940 | 4200 | 4535 | |
| $dK_6/K_6^{(1)}$ | Current sense ratio drift | $I_{OUT} = 20 \text{ A}; V_{SENSE} = 4 \text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | -4 | | 4 | % |
| $dK/K_{bulb1(TOT)}^{(1)}$ | Current sense ratio drift | $I_{OUT} = 1.6 \text{ A to } 4.2 \text{ A};$ $I_{OUTCAL} = 3 \text{ A}; V_{SENSE} = 2 \text{ V}$ | -15 | | 50 | % |
| $dK/K_{bulb2(TOT)}^{(1)}$ | Current sense ratio drift | $I_{OUT} = 0.6 \text{ A to } 2.4 \text{ A};$ $I_{OUTCAL} = 1.2 \text{ A}; V_{SENSE} = 2 \text{ V}$ | -30 | | 25 | % |
| I_{SENSE0} | Analog sense leakage current | $I_{OUT} = 0 \text{ A}; V_{SENSE} = 0 \text{ V};$ $V_{IN} = 0 \text{ V}; T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | 0 | | 1 | μA |
| | | $I_{OUT} = 0 \text{ A}; V_{SENSE} = 0 \text{ V};$ $V_{IN} = 5 \text{ V}; T_j = -40^\circ\text{C to } 150^\circ\text{C}$ | 0 | | 2 | |

Table 9. Current sense ($8\text{ V} < V_{CC} < 36\text{ V}$) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|--|--|------|------|------|---------------|
| V_{SENSE} | Max analog sense output voltage | $I_{OUT} = 20\text{ A}$; $R_{SENSE} = 3.9\text{ K}\Omega$ | 5 | | | V |
| V_{SENSEH} | Analog sense output voltage in fault condition ⁽²⁾ | $V_{CC} = 24\text{ V}$; $R_{SENSE} = 3.9\text{ K}\Omega$ | | 8 | | V |
| I_{SENSEH} | Analog sense output current in fault condition ⁽²⁾ | $V_{CC} = 24\text{ V}$; $V_{SENSE} = 5\text{ V}$ | | 9 | 12 | mA |
| $t_{DSENSE2H}$ | Delay response time from rising edge of INPUT pin | $V_{SENSE} < 4\text{ V}$; $0.5\text{ A} < I_{OUT} < 20\text{ A}$; $I_{SENSE} = 90\%$ of $I_{SENSE\text{ max}}$ (see Figure 7) | | 300 | 600 | μs |
| $\Delta t_{DSENSE2H}$ | Delay response time between rising edge of output current and rising edge of current sense | $V_{SENSE} < 4\text{ V}$; $I_{SENSE} = 90\%$ of $I_{SENSE\text{ MAX}}$; $I_{OUT} = 90\%$ of $I_{OUT\text{ MAX}}$ $I_{OUT\text{ MAX}} = 5\text{ A}$ (see Figure 10) | | | 450 | μs |
| $t_{DSENSE2L}$ | Delay response time from falling edge of INPUT pin | $V_{SENSE} < 4\text{ V}$; $0.5\text{ A} < I_{OUT} < 20\text{ A}$; $I_{SENSE} = 10\%$ of $I_{SENSE\text{ max}}$ (see Figure 7) | | 5 | 20 | μs |

- Parameter guaranteed by design; it is not tested.
- Fault condition includes: power limitation, overtemperature and open load in OFF-state condition.

Table 10. Openload detection ($FR_Stby = 5\text{ V}$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|---|--|------|------|------|---------------|
| V_{OL} | Openload Off State voltage detection threshold | $V_{IN} = 0\text{ V}$; $8\text{ V} < V_{CC} < 36\text{ V}$ | 2 | | 4 | V |
| t_{DSTKON} | Output short circuit to VCC detection delay at turn off | See Figure 8 . | 180 | | 1800 | μs |
| $I_{L(off2)}$ | Off state output current at $V_{OUT} = 4\text{ V}$ | $V_{IN} = 0\text{ V}$; $V_{SENSE} = 0\text{ V}$; V_{OUT} rising from 0 V to 4 V | -120 | | 0 | μA |
| t_{d_vol} | Delay response from output rising edge to V_{SENSE} rising edge in openload | $V_{OUT} = 4\text{ V}$; $V_{IN} = 0\text{ V}$; $V_{SENSE} = 90\%$ of V_{SENSEH} ; $R_{SENSE} = 3.9\text{ K}\Omega$ | | | 20 | μs |
| t_{DFRSTK_ON} | Output short circuit to VCC detection delay at FR_Stby activation | See Figure 6 ; Input _{1,2} = low | | | 50 | μs |

Figure 6. Output stuck to V_{CC} detection delay time at FR_Stby activation

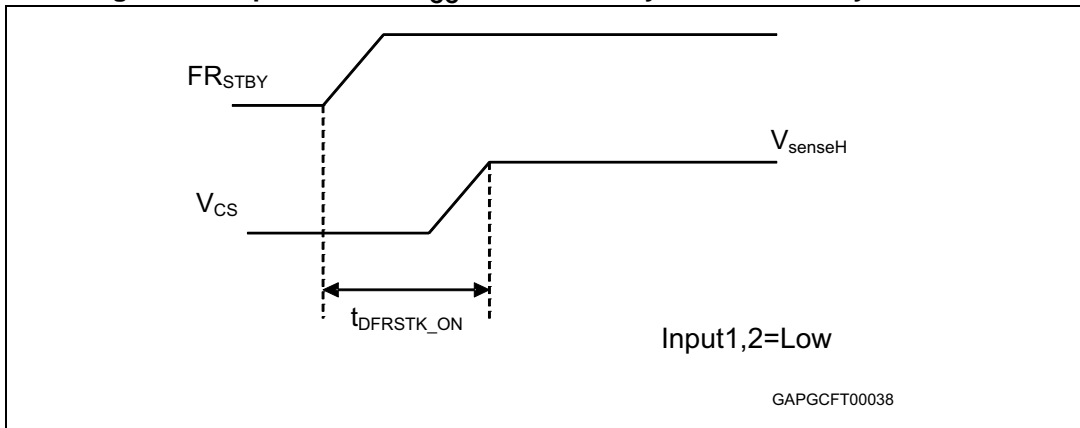


Figure 7. Current sense delay characteristics

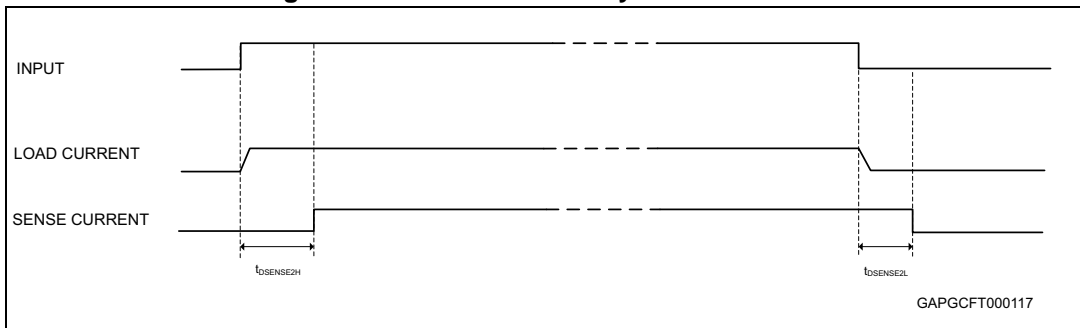


Figure 8. Open-load off-state delay timing

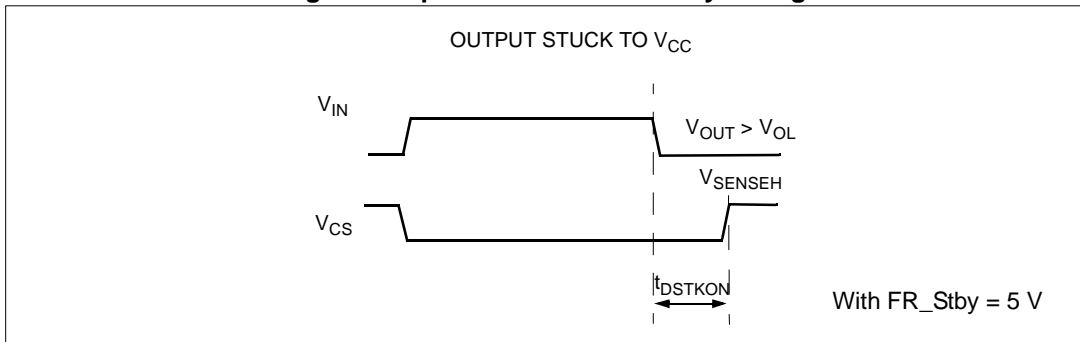


Figure 9. Switching characteristics

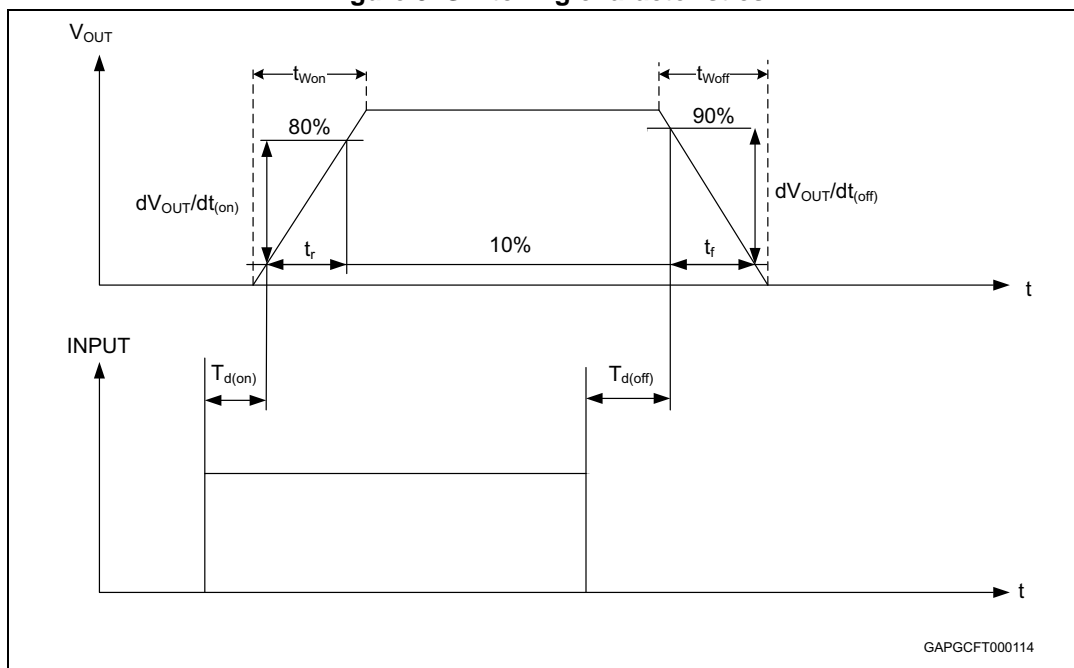


Figure 10. Delay response time between rising edge of output current and rising edge of current sense

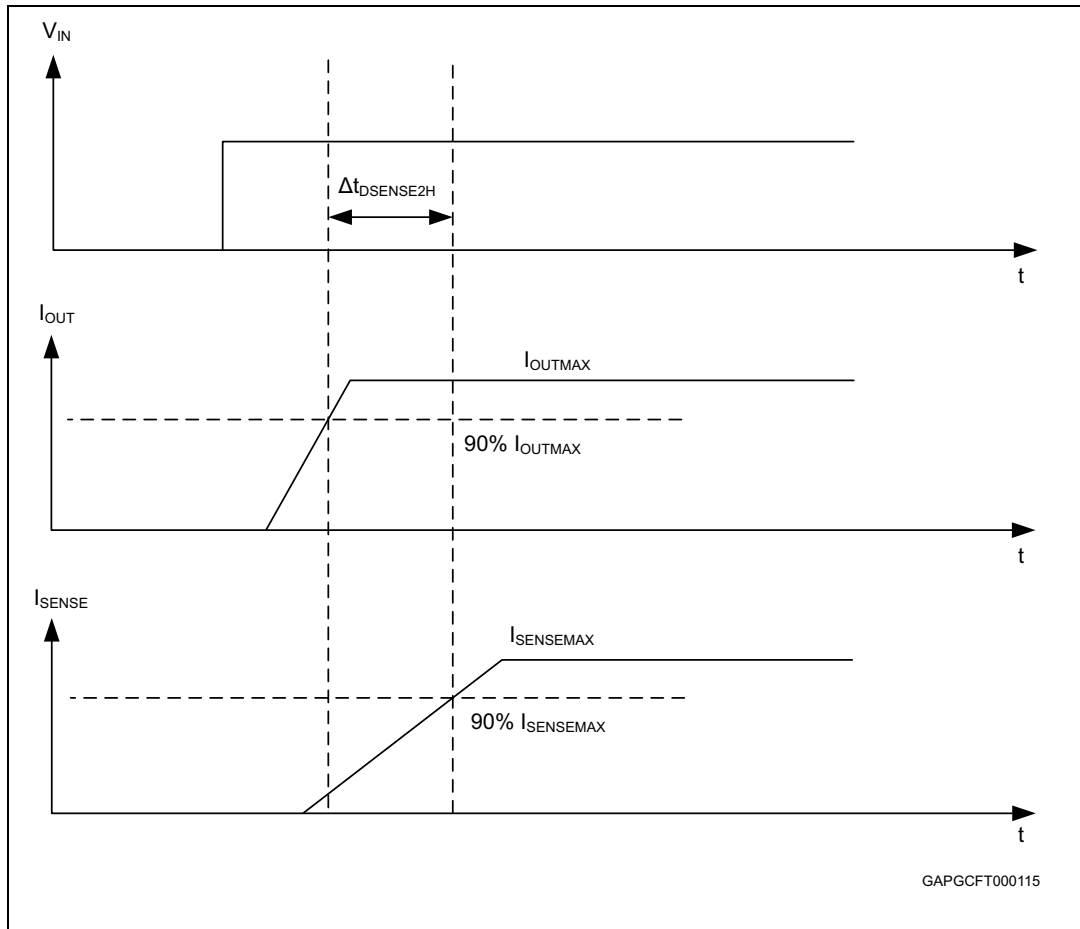


Figure 11. Output voltage drop limitation

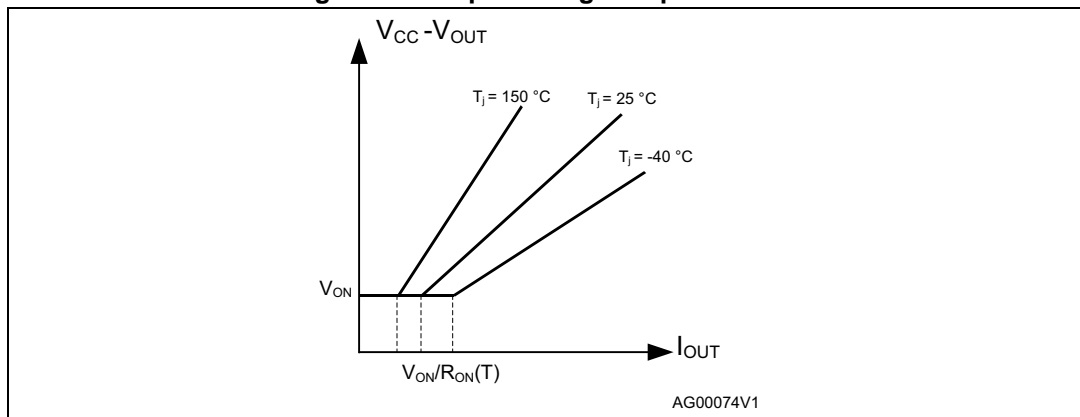


Figure 12. Device behavior in overload condition

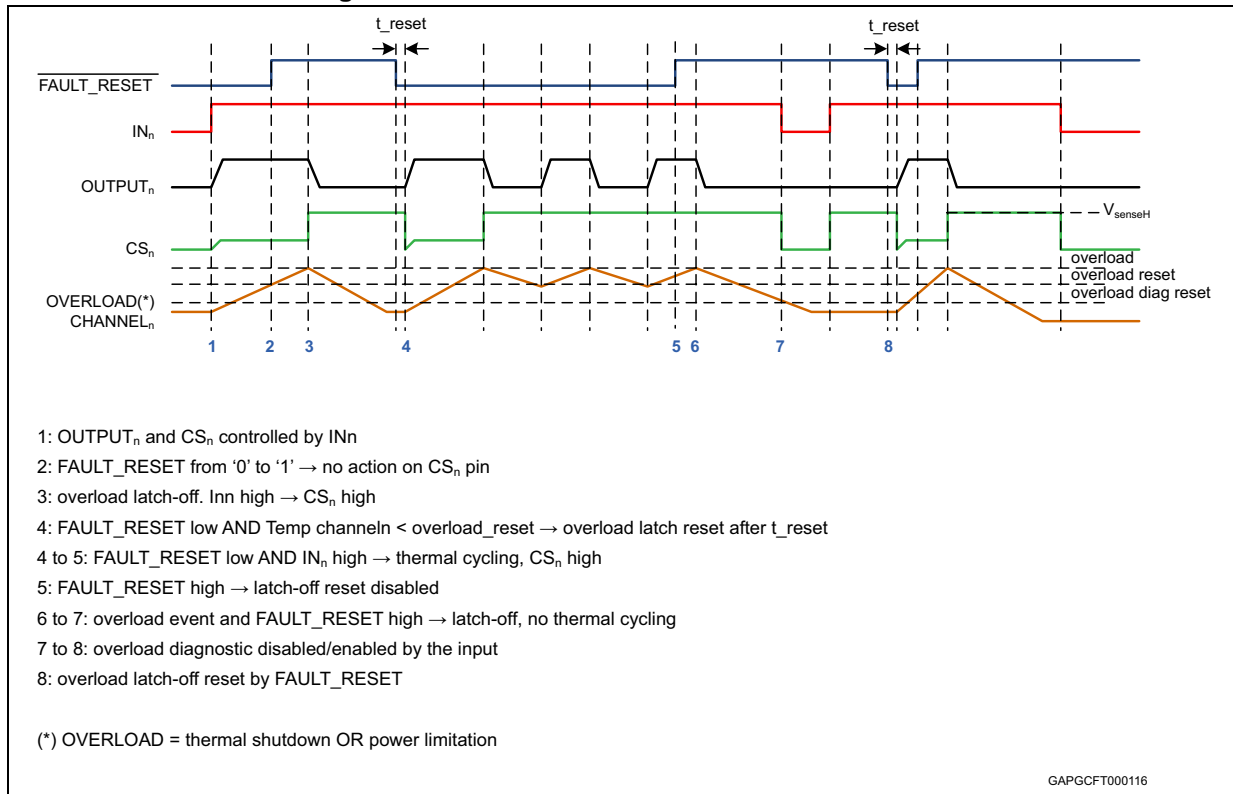


Table 11. Truth table

| Conditions | Fault reset standby | Input | Output | Sense |
|------------------------------------|---------------------|--------|--------------------|--|
| Standby | L | L | X | 0 |
| Normal operation | X | L | L | 0 |
| | X | H | H | Nominal |
| Overload | X | L | L | 0 |
| | X | H | H | > Nominal |
| Overtemperature / short to ground | X | L | L | 0 |
| | L H | H H | Cycling Latched | V _{SENSEH} V _{SENSEH} |
| Undervoltage | X | X | L | 0 |
| Short to V _{BAT} | L | L | H | 0 |
| | H X | L H | H H | V _{SENSEH} < Nominal |
| Open load Off-state (with pull-up) | L | L | H | 0 |
| | H | L | H | V _{SENSEH} |
| | X | H | H | 0 |
| Negative output voltage clamp | X | L | Negative | 0 |

Table 12. Electrical transient requirements (part 1)

| ISO 7637-2: 2004(E) Test pulse | Test levels ⁽¹⁾ | | Number of pulses or test times | Burst cycle/pulse repetition time | | Delays and impedance |
|--------------------------------------|----------------------------|---------|--------------------------------|-----------------------------------|--------|----------------------|
| | III | IV | | | | |
| 1 | - 450 V | - 600 V | 5000 pulses | 0.5 s | 5 s | 1 ms, 50 Ω |
| 2a | + 37 V | + 50 V | 5000 pulses | 0.2 s | 5 s | 50 μs, 2 Ω |
| 3a | - 150 V | - 200 V | 1h | 90 ms | 100 ms | 0.1 μs, 50 Ω |
| 3b | + 150 V | + 200 V | 1h | 90 ms | 100 ms | 0.1 μs, 50 Ω |
| 4 | - 12 V | - 16 V | 1 pulse | | | 100 ms, 0.01 Ω |
| 5b ⁽²⁾ | + 123 V | + 174 V | 1 pulse | | | 350 ms, 1 Ω |

1. The above test levels must be considered referred to $V_{CC} = 24.5$ V except for pulse 5b
2. Valid in case of external load dump clamp: 58 V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

| ISO 7637-2: 2004(E) Test pulse | Test level results | |
|--------------------------------------|--------------------|------------------|
| | III | IV |
| 1 | C | C ⁽¹⁾ |
| 2a | C | C |
| 3a | C | C |
| 3b ⁽²⁾ | E | E |
| 3b ⁽³⁾ | C | C |
| 4 | C | C |
| 5b ⁽⁴⁾ | C | C |

1. With $R_{load} < 24\Omega$.
2. Without capacitor between V_{CC} and GND.
3. With 10 nF between V_{CC} and GND.
4. External load dump clamp, 58 V maximum, referred to ground.

Table 14. Electrical transient requirements (part 3)

| Class | Contents |
|-------|--|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

2.4 Electrical characteristics curves

Figure 13. Off-state output current

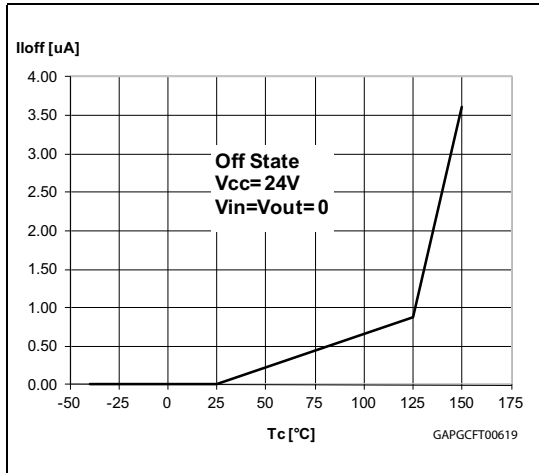


Figure 14. High level input current

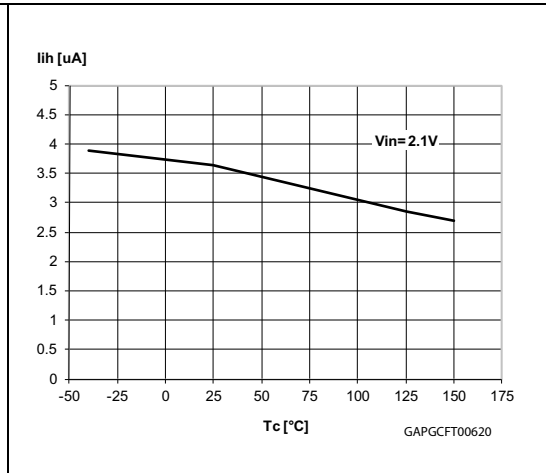


Figure 15. Input clamp voltage

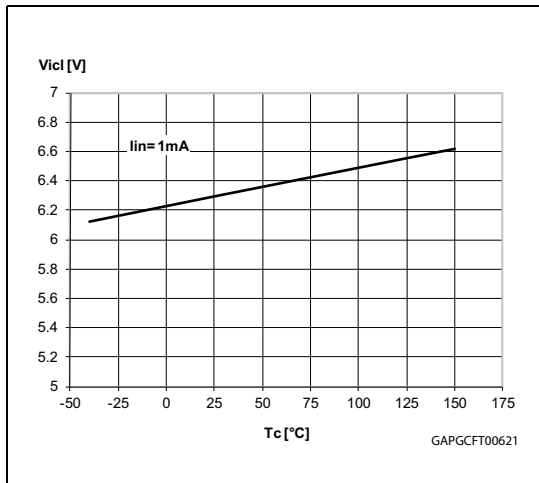


Figure 16. Input low level voltage

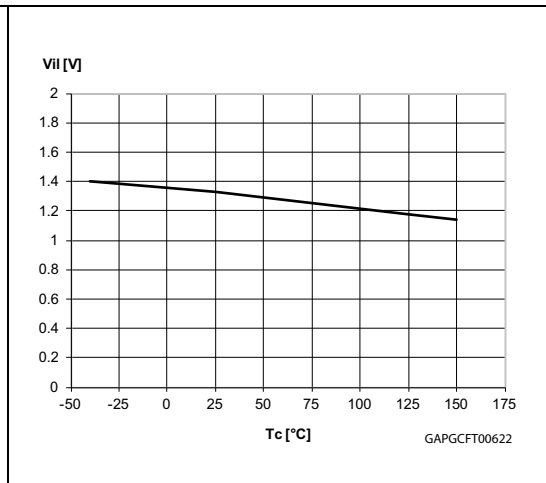


Figure 17. Input high level voltage

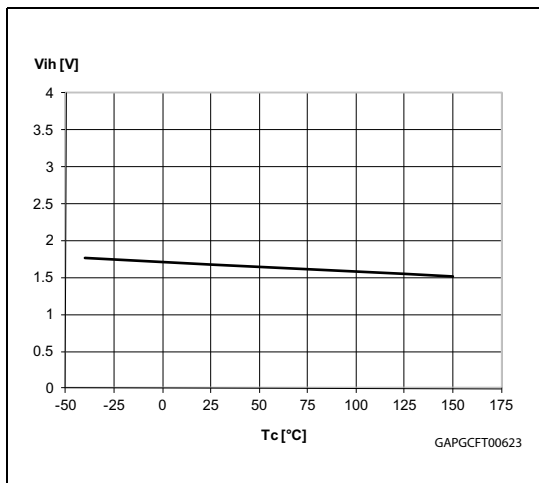


Figure 18. Input hysteresis voltage

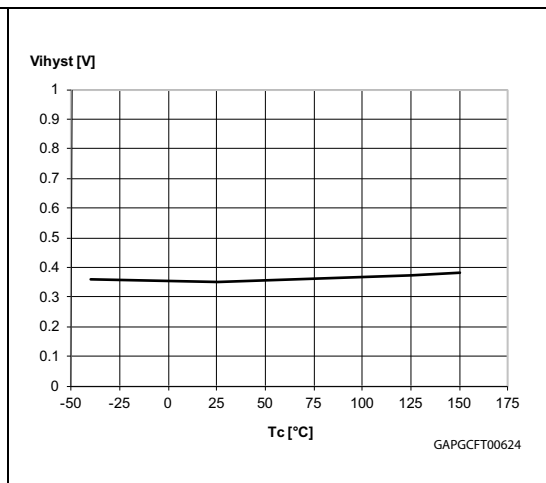


Figure 19. On-state resistance vs T_{case}

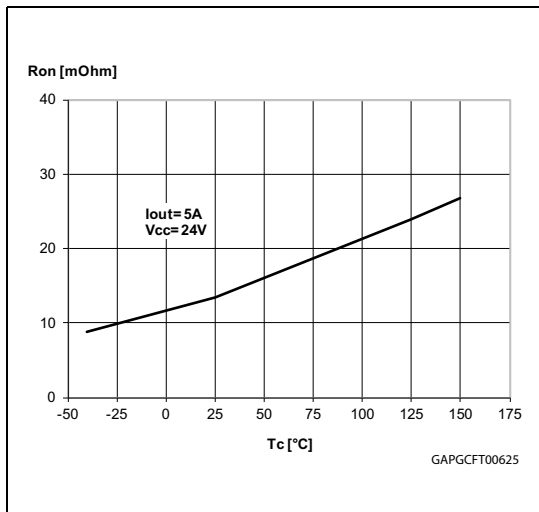


Figure 20. On-state resistance vs V_{CC}

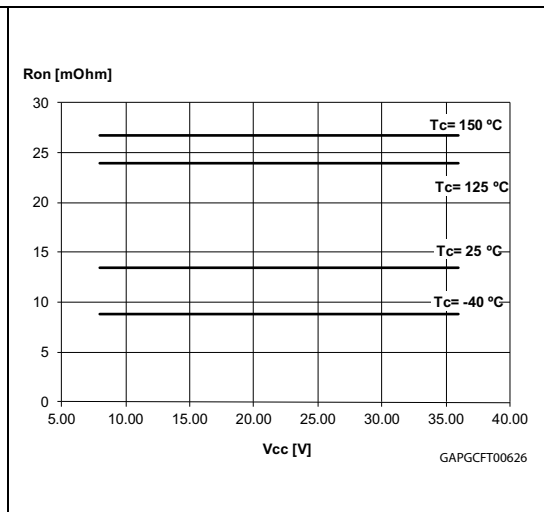


Figure 21. I_{LIMH} vs T_{case}

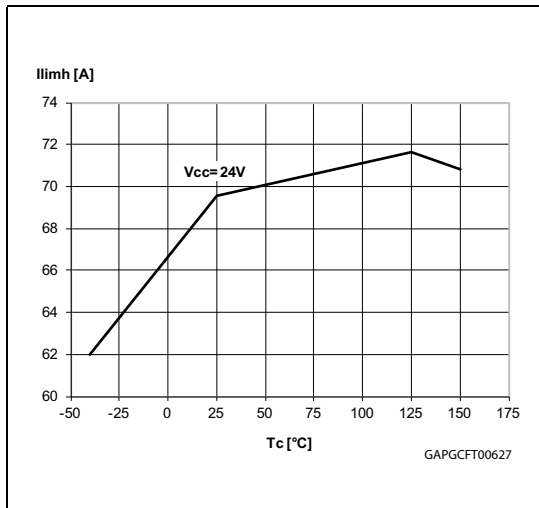


Figure 22. Turn-on voltage slope

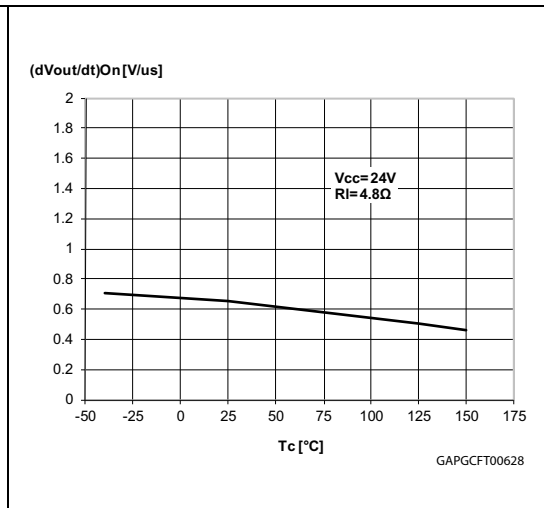
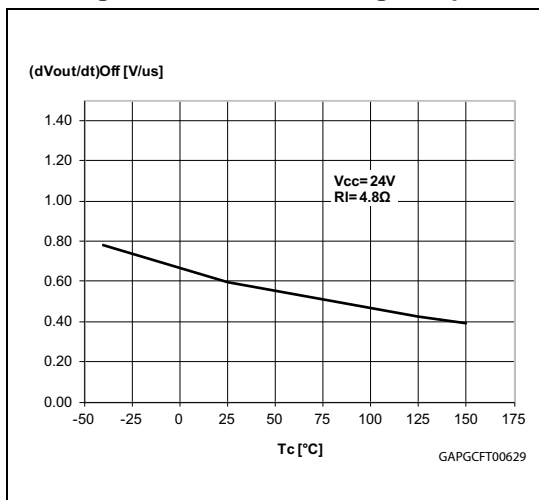
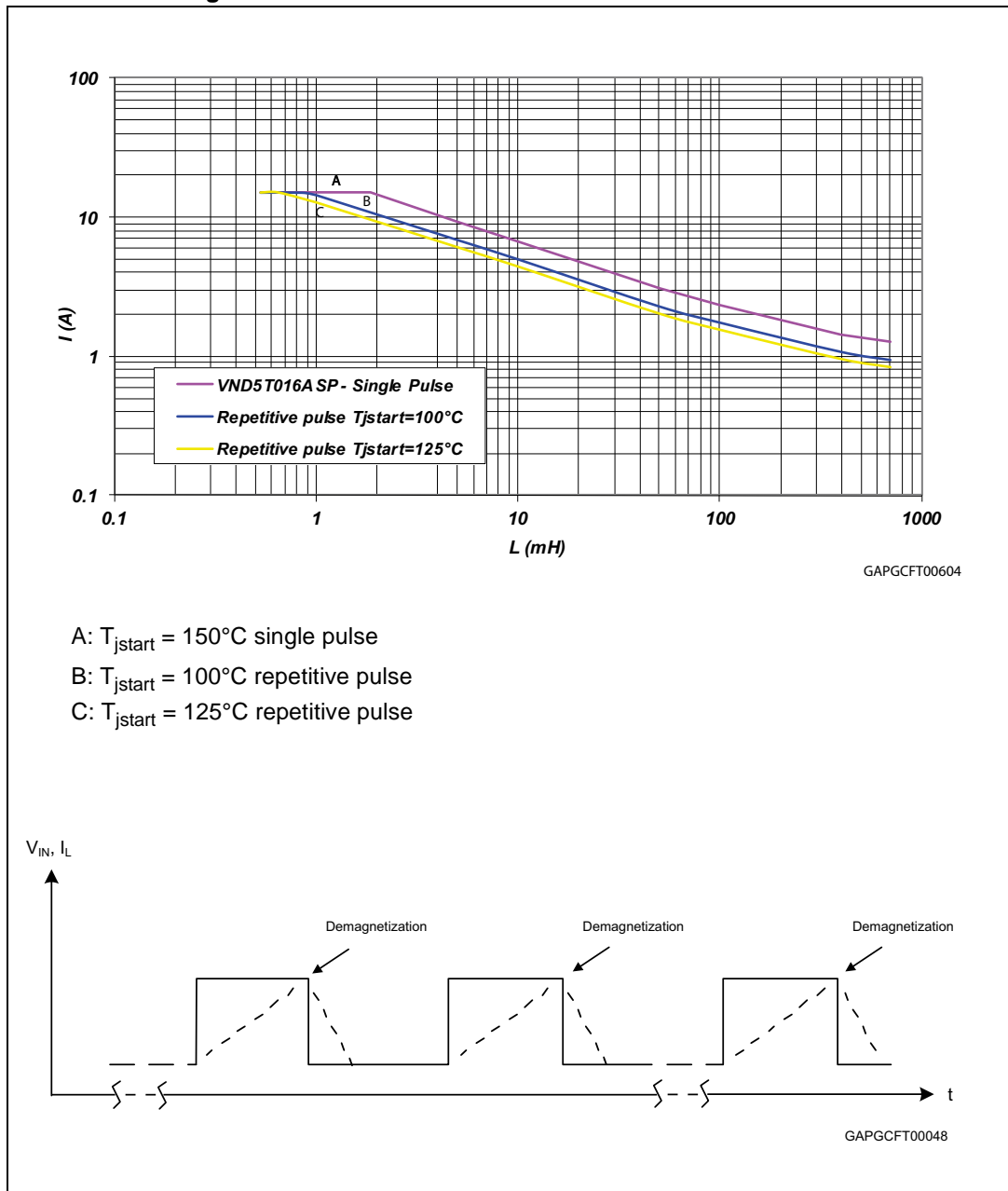


Figure 23. Turn-off voltage slope



2.5 Maximum demagnetization energy ($V_{CC} = 24\text{ V}$)

Figure 24. Maximum turn-off current versus inductance



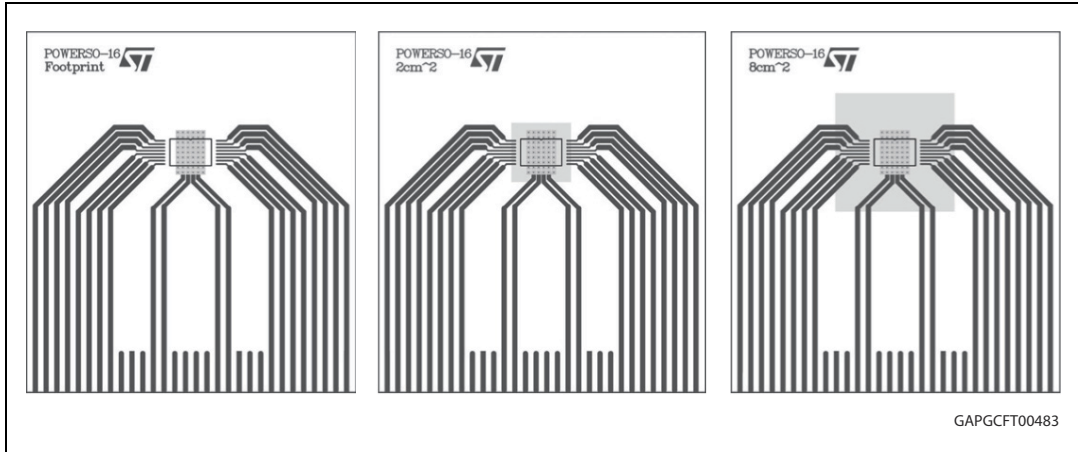
- A: $T_{jstart} = 150^{\circ}\text{C}$ single pulse
- B: $T_{jstart} = 100^{\circ}\text{C}$ repetitive pulse
- C: $T_{jstart} = 125^{\circ}\text{C}$ repetitive pulse

Note: Values are generated with $R_L = 0\ \Omega$. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3 Package and PCB thermal data

3.1 PowerSO-16 thermal data

Figure 25. PowerSO-16 PC board



1. Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10%; board double layer; board dimension 77 mm x 86 mm; board material FR4; Cu thickness 70 μ m (front and back side); thermal vias separation 1.2 mm; thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm).

Figure 26. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

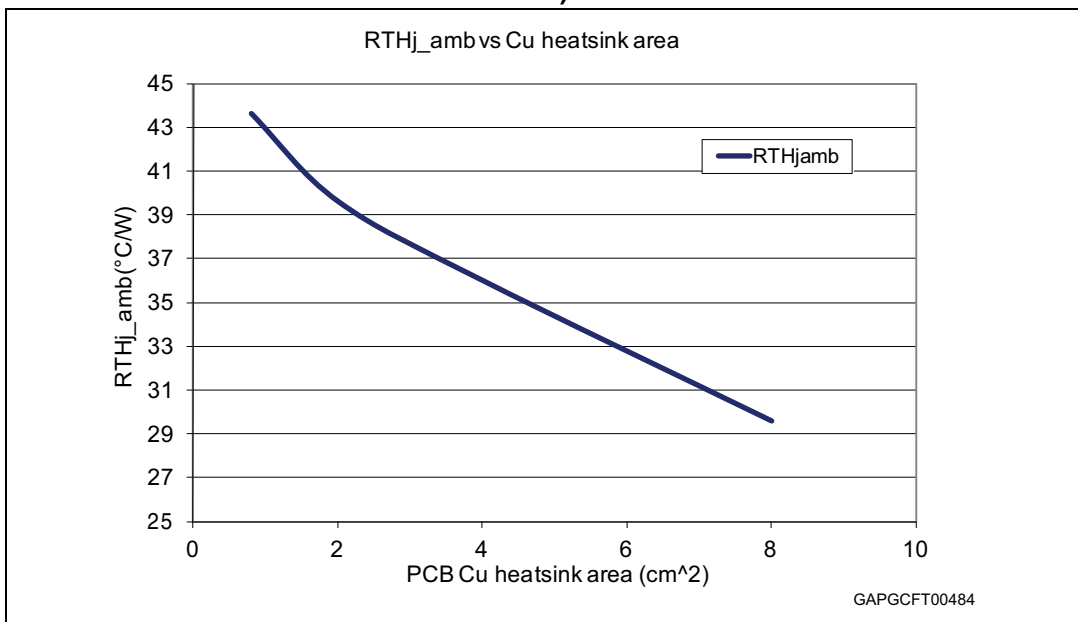


Figure 27. PowerSO-16 thermal impedance junction ambient single pulse (one channel ON)

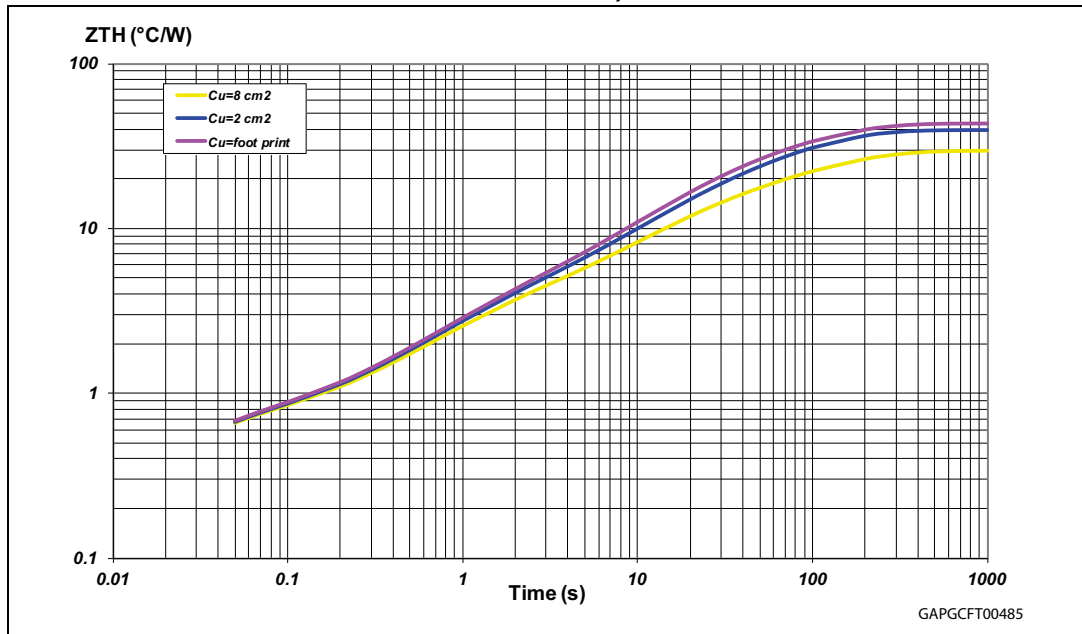
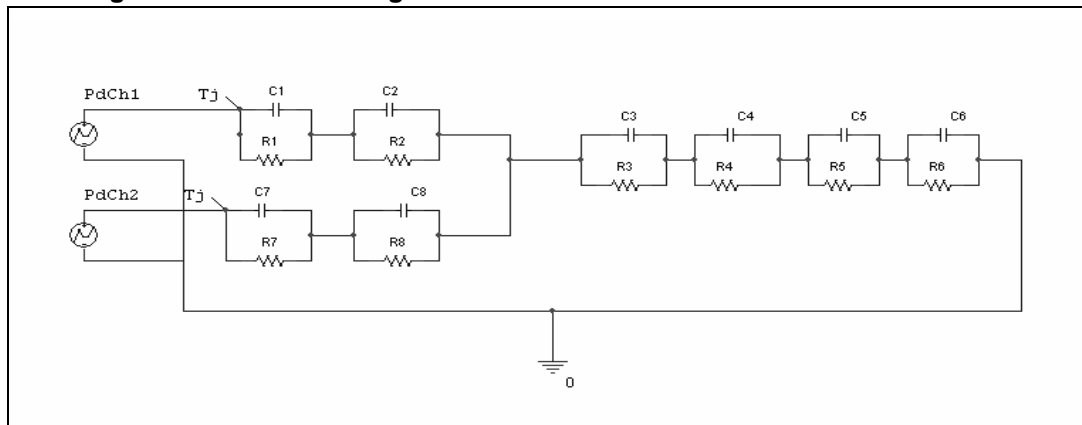


Figure 28. Thermal fitting model of a double channel HSD in PowerSO-16



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 15. Thermal parameters

| Area/island (cm ²) | Footprint | 2 | 8 |
|--------------------------------|-----------|----|----|
| R1 = R7 (°C/W) | 0.1 | | |
| R2 = R8 (°C/W) | 0.5 | | |
| R3 (°C/W) | 2 | | |
| R4 (°C/W) | 7 | | |
| R5 (°C/W) | 12 | 12 | 8 |
| R6 (°C/W) | 22 | 18 | 12 |
| C1 = C7 (W.s/°C) | 0.01 | | |
| C2 = C8 (W.s/°C) | 0.05 | | |
| C3 (W.s/°C) | 0.5 | | |
| C4 (W.s/°C) | 2 | | |
| C5 (W.s/°C) | 3 | 4 | 7 |
| C6 (W.s/°C) | 5 | 6 | 12 |

4 Package information

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 PowerSO-16 mechanical data

Figure 29. PowerSO-16 package dimensions

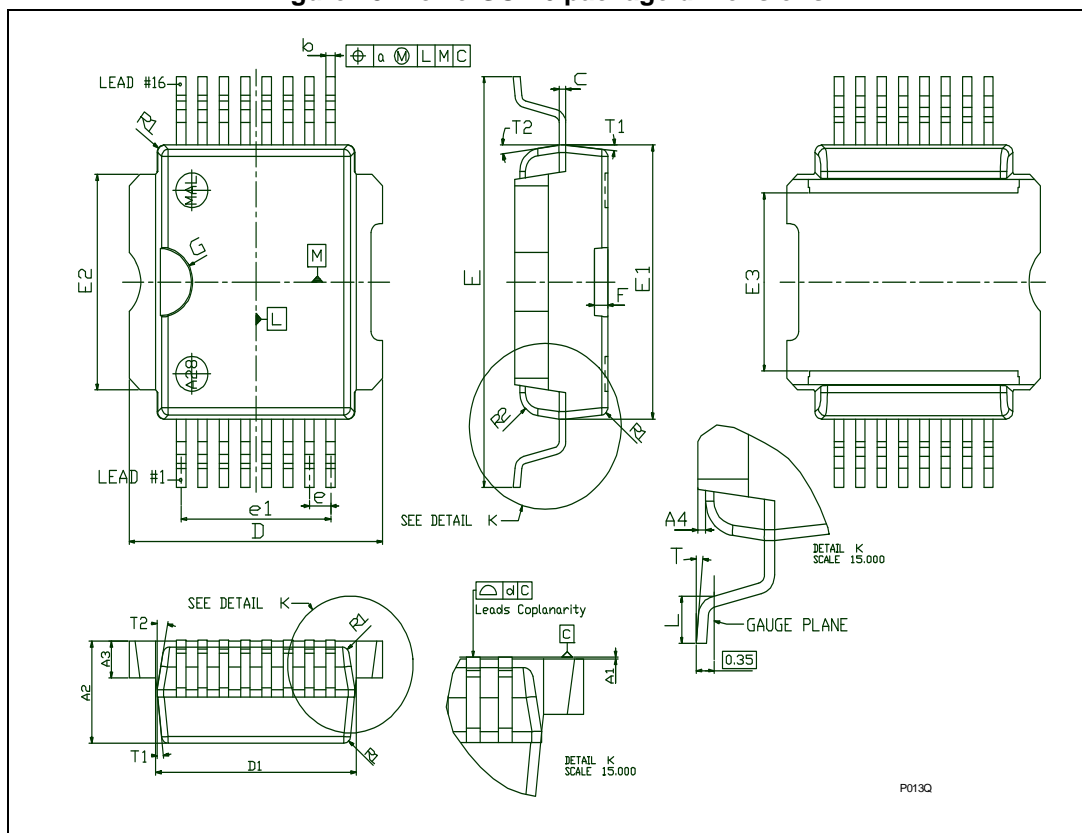


Table 16. PowerSO-16 mechanical data

| Dim. | mm | | |
|----------------|------------|------|-------|
| | Min. | Typ. | Max. |
| A1 | 0 | 0.05 | 0.1 |
| A2 | 3.4 | 3.5 | 3.6 |
| A3 | 1.2 | 1.3 | 1.4 |
| A4 | 0.15 | 0.2 | 0.25 |
| a | | 0.2 | |
| b | 0.27 | 0.35 | 0.43 |
| c | 0.23 | 0.27 | 0.32 |
| D | 9.4 | 9.5 | 9.6 |
| D1 | 7.4 | 7.5 | 7.6 |
| d | 0 | 0.05 | 0.1 |
| E (1) | 13.85 | 14.1 | 14.35 |
| E1 | 9.3 | 9.4 | 9.5 |
| E2 | 7.3 | 7.4 | 7.5 |
| E3 | 5.9 | 6.1 | 6.3 |
| e | | 0.8 | |
| e1 | | 5.6 | |
| F | | 0.5 | |
| G | | 1.2 | |
| L | 0.8 | 1 | 1.1 |
| R1 | | | 0.25 |
| R2 | | 0.8 | |
| T | 2° | 5° | 8° |
| T1 | 6° (typ.) | | |
| T2 | 10° (typ.) | | |
| Package weight | (typ.) | | |

4.3 Packing information

Figure 30. PowerSO-16 tube shipment (no suffix)

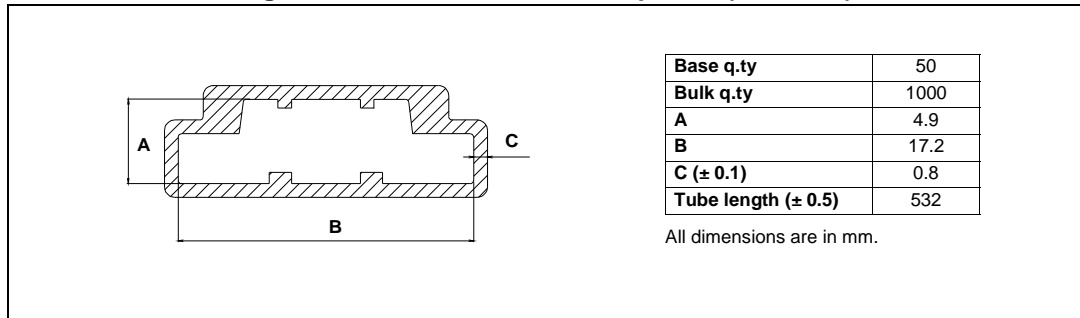


Figure 31. PowerSO-16 tape and reel shipment (suffix "TR")

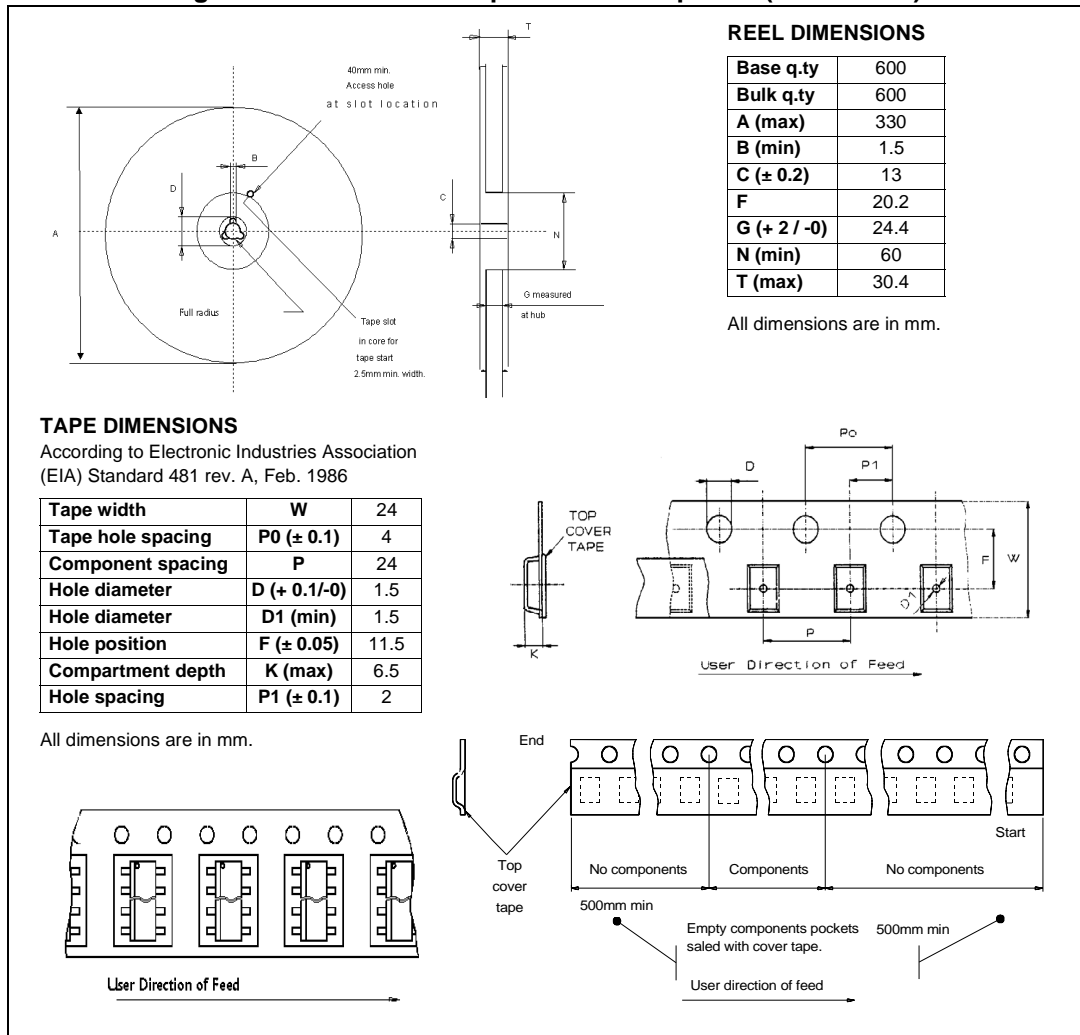
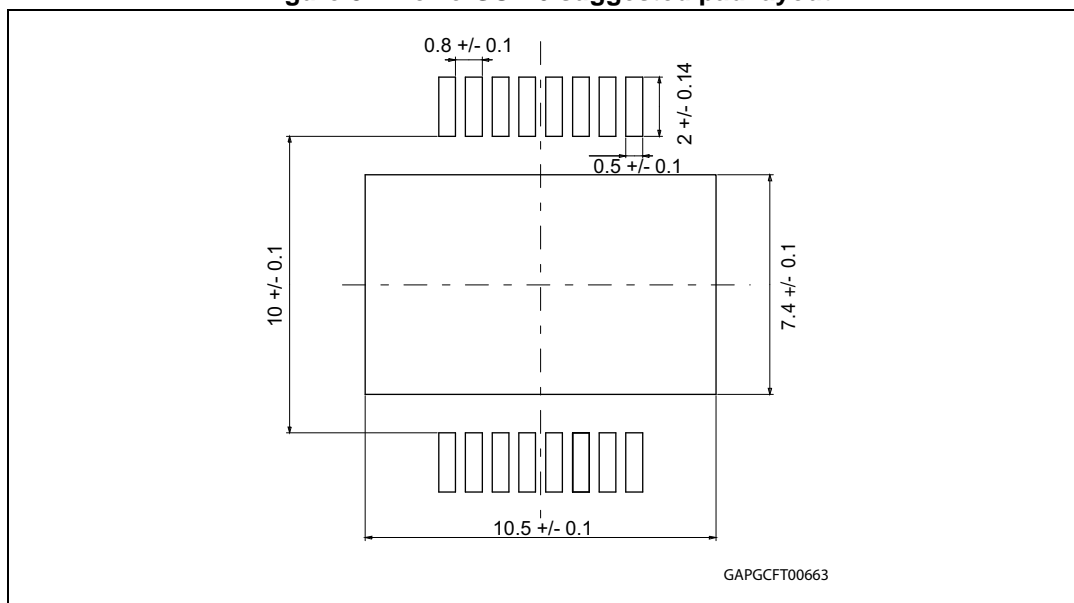


Figure 32. PowerSO-16 suggested pad layout



5 Order codes

Table 17. Device summary

| Package | Order codes | |
|------------|---------------|-----------------|
| | Tube | Tape and reel |
| PowerSO-16 | VND5T016ASP-E | VND5T016ASPTR-E |

6 Revision history

Table 18. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 15-Feb-2012 | 1 | Initial release. |
| 13-Apr-2012 | 2 | Updated <i>Table</i> : <i>Table 9: Current sense (8 V < VCC < 36 V):</i> – renamed dK_{led}/K_{led} in $dK_{led}/K_{led(TOT)}$, dK/K_{bulb1} in $dK/K_{bulb1(TOT)}$ and dK/K_{bulb2} in $dK/K_{bulb2(TOT)}$ – $dK/K_{bulb1(TOT)}$, $dK/K_{bulb2(TOT)}$: updated test condition |
| 18-Sep-2013 | 3 | Updated disclaimer. |
| 16-Feb-2016 | 4 | <i>Table 4: Thermal data:</i> – $R_{thj-case}$: updated value |

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