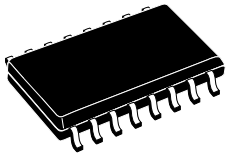
ST8034T, ST8034AT, ST8034P, ST8034C

16-pin smartcard interfaces

Datasheet - production data



SO16 3.9 x 9.9 mm

QFN16 3 x 3 mm

Features

- Complete smartcard interface
- ISO 7816 and EMV™ 4.3 payment systems compatible
- One protected half-duplex bidirectional buffered I/O line to the smartcard
- 5 V or 3 V (or 1.8 V in case of ST8034P) selectable smartcard supply voltage (V_{CC}). Ensures controlled V_{CC} rise and fall times and provides smart overload detection with glitch immunity.
- Optional chip select function allows the device interface to be isolated from the host microcontroller signals - allows parallel combination of the card interface devices (ST8034C)
- Card clock generation by integrated crystal oscillator or from external clock source
- Card clock frequency up to 20 MHz, programmable by CLKDIV pin, with synchronous frequency changes
- Optional VCC_SEL input for pin-controlled selection of V_{CC}; 5 V or 3 V or 1.8 V (ST8034P)
- Automatic card activation and deactivation sequences initiated by the microcontroller
- Emergency deactivation sequences initiated by a card supply short-circuit, card take-off, falling V_{DD}, V_{DDP}, or $V_{DD(INTF)}$ or by the interface device overheating
- Voltage supply supervisors
  - With a fixed threshold (V_{DD}, V_{DDP}, and $V_{DD(INTF)}$)
  - Optionally with an external resistor divider to set the $V_{DD(INTF)}$ threshold (PORADJ pin; ST8034P and ST8034C)
- Multipurpose card status signal $\overline{OFF}$
- Non-inverted card reset pin RST driven by the RSTIN input
- Thermal and short-circuit protection of all card contacts
- Card presence detection contacts debounced
- Enhanced card side ESD protection of 8 kV
- Common SO16 3.9 x 9.9 mm body or a space-saving QFN16 3 x 3 mm package
- Temperature range -25 to +85 °C

Applications

Smartcard readers for

- Set-top boxes
- Pay-TV
- Identification
- Banking
- Tachographs

Contents

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1 Description

The ST8034T/ST8034AT/ST8034P/ST8034C devices are complete low-cost analog interfaces for asynchronous and synchronous smartcards operating at a supply voltage of 5 V or 3 V (or even 1.8 V in the case of ST8034P).

The ST8034T/ST8034AT/ST8034P/ST8034C devices can be placed between the card and the microcontroller to provide all supply, protection, detection and control functions, with just a few external components.

Table 1. Device summary

Order code	PORADJ	CLKDIV	CLKIN	External crystal	V_{CC} selection pin 5/3.0/1.8 V	Chip select	Package	Shipment	Package topmark
ST8034TDT		v		v			SO16 (3.9 x 9.9 mm)	Tape and reel	ST8034TDT
ST8034ATDT		v		v			SO16 (3.9 x 9.9 mm)	Tape and reel	ST8034ATDT
ST8034PQR	v		v		v		QFN16 (3 x 3 mm)	Tape and reel	034P
ST8034CQR	v		v			v	QFN16 (3 x 3 mm)	Tape and reel	034C

2 Block diagrams

Figure 1. Block diagram ST8034T and ST8034AT

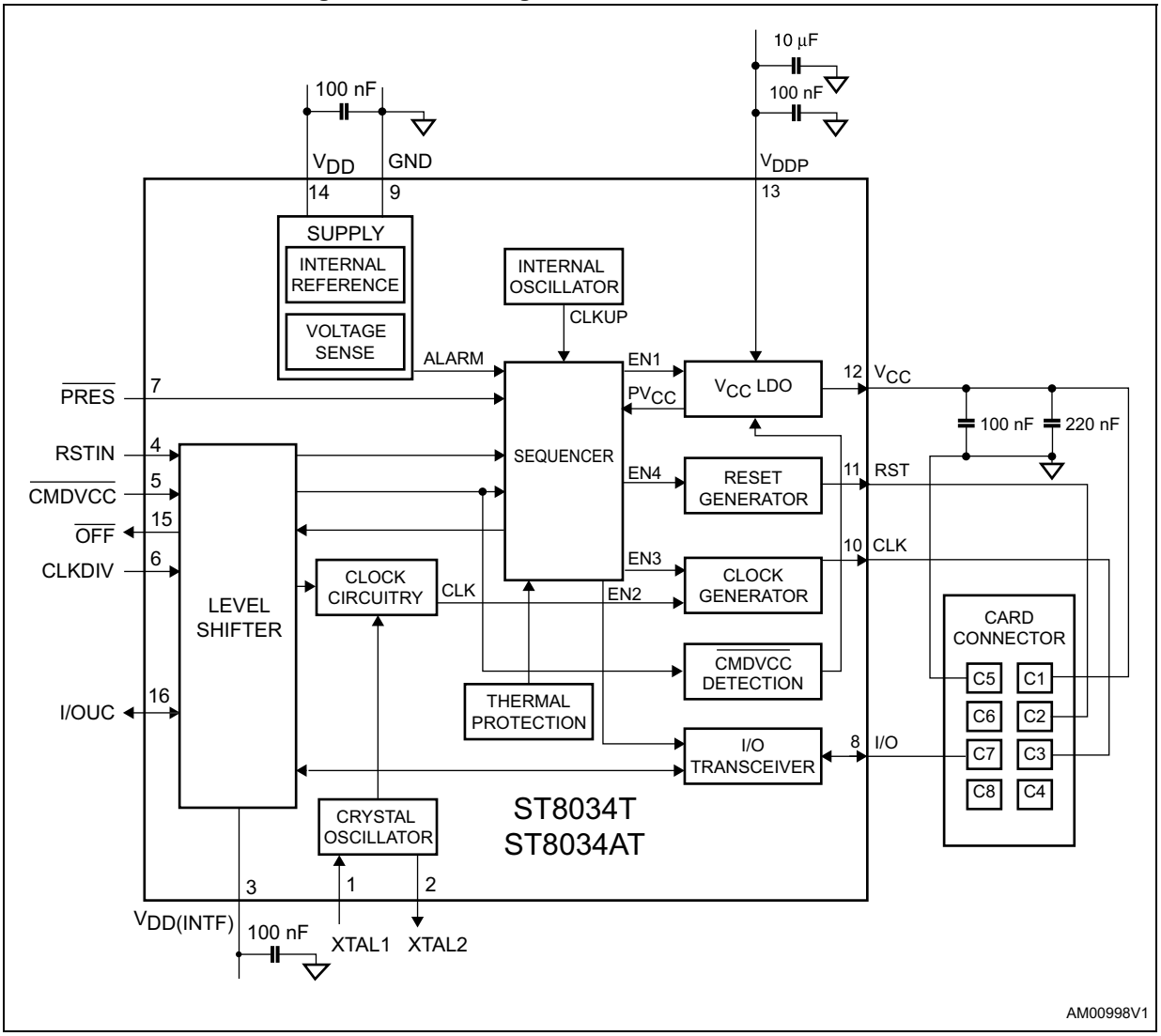
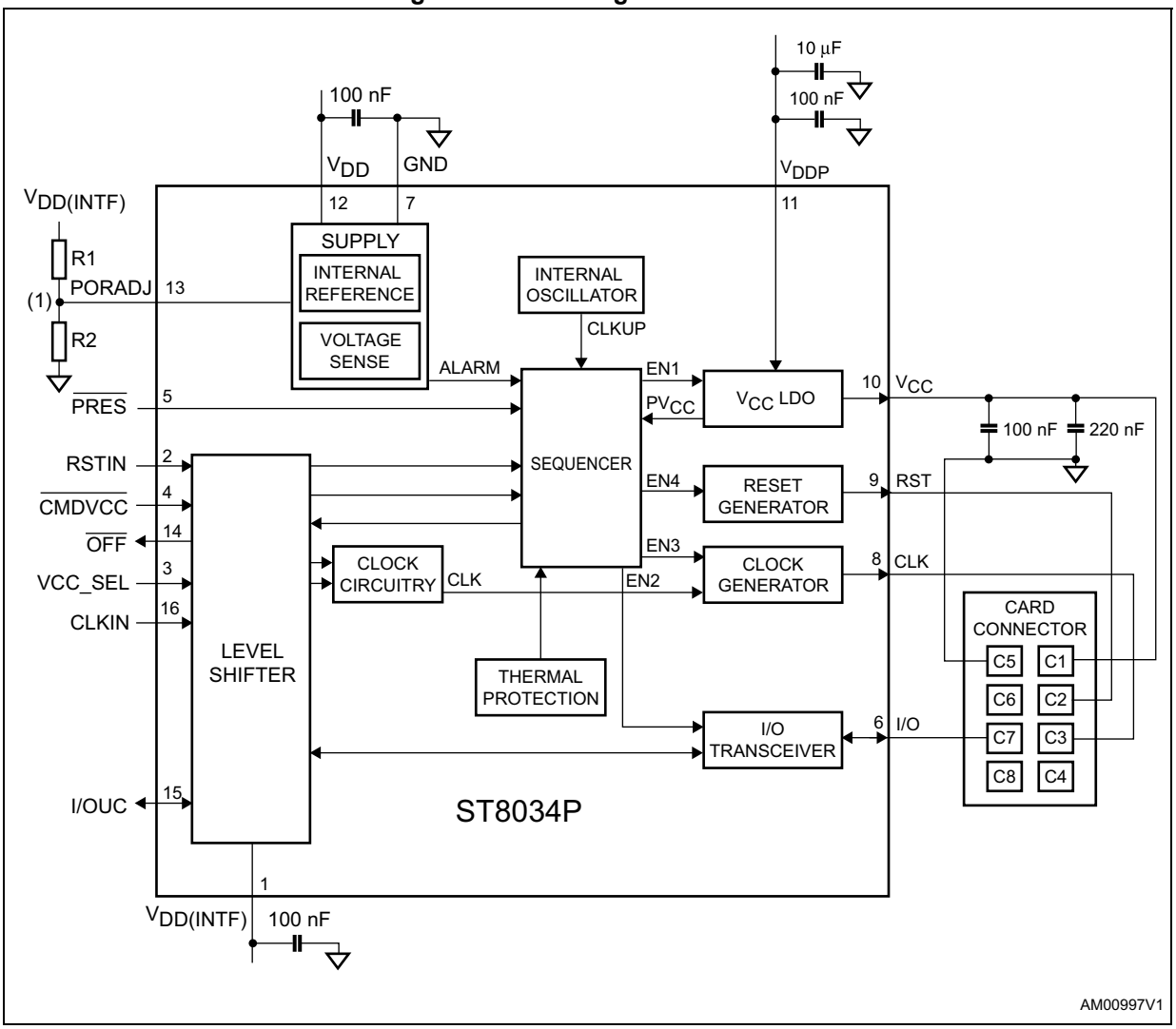
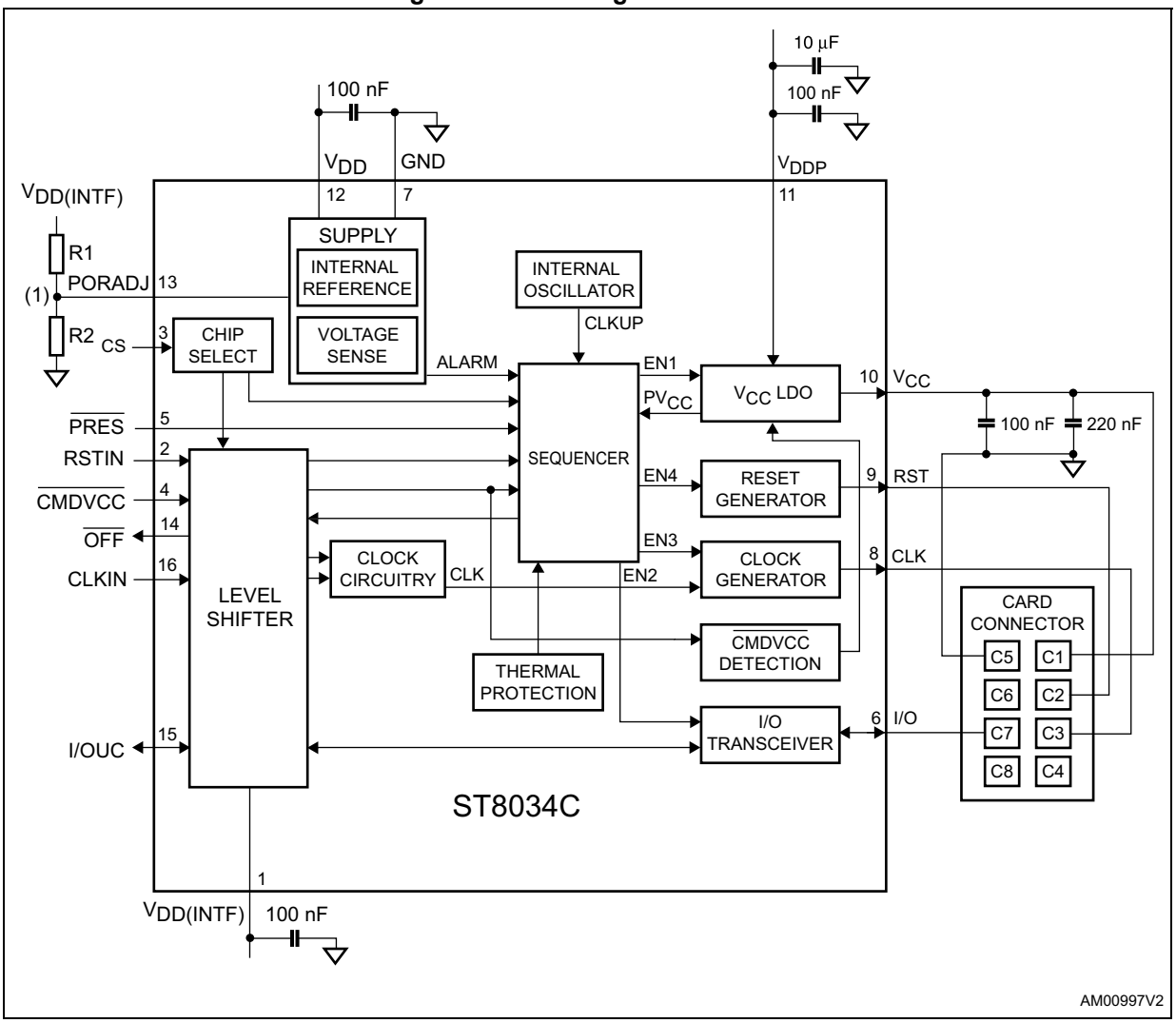


Figure 2. Block diagram ST8034P



1. Optional external resistor divider. If not used, connect PORADJ pin to $V_{DD(INTF)}$ for a direct $V_{DD(INTF)}$ voltage monitoring.

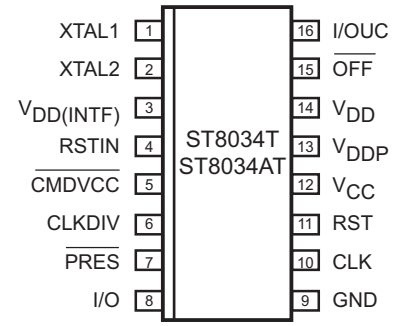
Figure 3. Block diagram ST8034C



1. Optional external resistor divider. If not used, connect PORADJ pin to $V_{DD(INTF)}$ for a direct $V_{DD(INTF)}$ voltage monitoring.

3 Pin description

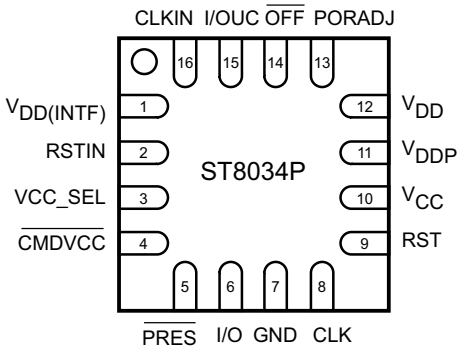
Figure 4. Pin connections ST8034T and ST8034AT, top view



SO16 3.9 x 9.9 mm

AM00999v2

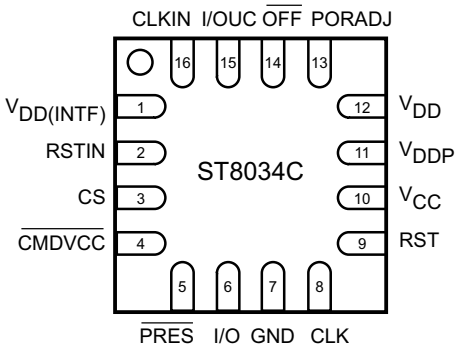
Figure 5. Pin connections ST8034P (options VCC_SEL and PORADJ pins), top-through view



QFN16 3 x 3 x 0.8 mm, 0.5 mm pitch. Thermal pad not connected.

AM00428V2

Figure 6. Pin connections ST8034C (options chip select and PORADJ pins), top-through view



QFN16 3 x 3 x 0.8 mm, 0.5 mm pitch. Thermal pad not connected.

AM00428V3

Table 2. Pin description ST8034T and ST8034AT

Pin number	Symbol	Ref. supply	Function
1	XTAL1	V_{DD}	Crystal or external clock input
2	XTAL2	V_{DD}	Crystal connection (leave this pin open if external clock is used)
3	$V_{DD(INTF)}$		Microcontroller interface supply voltage
4	RSTIN	$V_{DD(INTF)}$	Card reset input from microcontroller
5	$\overline{\text{CMDVCC}}$	$V_{DD(INTF)}$	Start activation sequence input (from microcontroller, active low)
6	CLKDIV	$V_{DD(INTF)}$	CLK frequency division control
7	$\overline{\text{PRES}}$	$V_{DD(INTF)}$	Card presence input (active low: $\overline{\text{PRES}}$ low = card is present). Debounced.
8	I/O	V_{CC}	Card input/output data line (C7); with internal 9 kΩ pull-up resistor to V_{CC}.
9	GND		Ground
10	CLK	V_{CC}	Clock to card (C3)
11	RST	V_{CC}	Card reset, output (C2)
12	V_{CC}		Supply voltage for the card, output (C1)
13	V_{DDP}		LDO supply voltage input (for V_{CC} generation)
14	V_{DD}		Logic supply voltage input
15	$\overline{\text{OFF}}$	$V_{DD(INTF)}$	Interrupt to microcontroller (active low output, with internal 20 kΩ pull-up resistor to $V_{DD(INTF)}$)
16	I/OUC	$V_{DD(INTF)}$	Microcontroller data I/O line (with internal 10 kΩ pull-up resistor connected to $V_{DD(INTF)}$)

Note: Difference between the ST8034T and ST8034AT is the clock frequency division control, see *Table 13 on page 25**.*

Table 3. Pin description ST8034P and ST8034C

Pin number	Symbol	Ref. supply	Function
1	$V_{DD(INTF)}$		Microcontroller interface supply voltage (input)
2	RSTIN	$V_{DD(INTF)}$	Card reset input from microcontroller
3	CS	$V_{DD(INTF)}$	Chip select input. CS = high => device is active, low => all microcontroller interface pins set to high impedance. (ST8034C)
	VCC_SEL	$V_{DD(INTF)}$	V_{CC} (card supply) selection input: logic high selects V_{CC} = 5 V, logic low selects V_{CC} = 3 V, left-floating selects V_{CC} = 1.8 V. (ST8034P)
4	$\overline{CMDVCC}$	$V_{DD(INTF)}$	Start activation sequence input (from microcontroller, active low)
5	$\overline{PRES}$	$V_{DD(INTF)}$	Card presence input (active low: $\overline{PRES}$ = low => card is present). Debounced.
6	I/O	V_{CC}	Card input/output data line (C7); with internal 9 kΩ pull-up resistor to V_{CC}
7	GND		Ground
8	CLK	V_{CC}	Clock to card (C3)
9	RST	V_{CC}	Card reset, output (C2)
10	V_{CC}		Supply voltage for the card, output (C1)
11	V_{DDP}		LDO supply voltage input (for V_{CC} generation)
12	V_{DD}		Control logic supply voltage input
13	PORADJ	$V_{DD(INTF)}$	Power-on reset threshold adjustment input
14	$\overline{OFF}$	$V_{DD(INTF)}$	Interrupt to microcontroller (active low output, with internal 20 kΩ pull-up resistor to $V_{DD(INTF)}$)
15	I/OUC	$V_{DD(INTF)}$	Microcontroller data I/O line (with internal 10 kΩ pull-up resistor connected to $V_{DD(INTF)}$)
16	CLKIN	$V_{DD(INTF)}$	External clock input

4 Maximum ratings

Table 4. Absolute maximum ratings(1), (2)

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage, logic	-0.3	6	V
V_{DDP}	Supply voltage, power	-0.3	6	V
$V_{DD(INTF)}$	Supply voltage, interface	-0.3	6	V
V_{IN}	Input voltage on XTAL1, XTAL2, RSTIN, I/OUC, CLKDIV, CS, VCC_SEL, CLKIN, PORADJ, CMDVCC, OFF, PRES, and I/O pins	-0.3	6	V
$V_{ESD\ (HBM)}$	Human body model (HBM) on card lines - I/O, RST, V_{CC}, CLK, and PRES pins	-8	8	kV
	Human body model (HBM), all other pins	-2	2	kV
$V_{ESD\ (MM)}$	Machine model (MM), all pins	-200	200	V
$V_{ESD\ (FCDM)}$	Field charged device model (FCDM), all pins	-500	500	V
P_{TOT}	Total power dissipation (T_A = -25 to +85 °C)		0.25	W
$T_{J(MAX)}$	Maximum operating junction temperature		125	°C
T_{STG}	Storage temperature range	-55	150	°C

1. Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
2. All card contacts are protected against short-circuit to any other card contact.

Table 5. Thermal data

Symbol	Parameter	Test conditions	Typ.	Unit
R_{THJA}	Thermal resistance junction-ambient temperature (multilayer test board - JEDEC standard)	SO16	87	°C/W
		QFN16	60	°C/W

Table 6. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
T_A	Ambient temperature range		-25	85	°C

5 Electrical characteristics

Electrical characteristics over recommended operating conditions

Table 7. Supply voltages

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
Device supply voltages						
V_{DD}	Supply voltage, logic		2.7	3.3	5.5(2)	V
V_{DDP}	Supply voltage, power	V_{CC} = 5 V	4.85	5	5.5	V
		V_{CC} = 3 V or 1.8 V	3	3.3	5.5	
$V_{DD(INTF)}$	Supply voltage, microcontroller interface		1.6	3.3	V_{DD} +0.3(3)	V
I_{DD}	Supply current, logic	Shutdown mode			35	µA
		Active mode			2	mA
I_{DDP}	Supply current, power	Shutdown mode, f_{XTAL} stopped			5	µA
		Active mode, $f_{CLK} = f_{XTAL}/2$, no I_{CC} load			1.5	mA
		Active mode, $f_{CLK} = f_{XTAL}/2$, I_{CC} = 65 mA			70	
$I_{DD(INTF)}$	Supply current, interface	Shutdown mode			6	µA
		Shutdown mode, ST8034P only			45	µA
Card supply voltage						
V_{CC}	Card supply voltage (output)(4)	Active mode, V_{CC} = 5 V, I_{CC} < 65 mA	4.75	5.0	5.25	V
		With current pulses of 40 nAs at I_{CC} < 200 mA, t < 400 ns(4)	4.65	5.0	5.25	
		Active mode, V_{CC} = 3 V, I_{CC} < 65 mA	2.85	3.05	3.15	
		With current pulses of 40 nAs at I_{CC} < 200 mA, t < 400 ns(4)	2.76		3.20	
		Active mode, V_{CC} = 1.8 V, I_{CC} < 65 mA	1.71	1.83	1.89	
		With current pulses of 15 nAs at I_{CC} < 200 mA, t < 400 ns(4)	1.66		1.94	
I_{CC}	Card supply current (refer also to *Table 11: Protection characteristics on page 21*)	V_{CC} = 5 V, 3 V or 1.8 V			65	mA
		V_{CC} shorted to GND	90	120	150	
C_{VCC}	V_{CC} decoupling capacitor(5)	V_{CC} to GND	160	320	530	nF
SR	V_{CC} slew rate (rising and falling)(5)	V_{CC} = 5 V	0.055	0.180	0.300	V/µs
		V_{CC} = 3 V	0.040	0.180	0.300	
		V_{CC} = 1.8 V	0.025	0.180	0.300	
$V_{CC(SHDN)}$	V_{CC} output voltage in shutdown mode	No load	-0.1		0.1	V
		I_{CC} = 1 mA	-0.1		0.3	

Table 7. Supply voltages (continued)

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
$I_{CC(SHDN)}$	V_{CC} output current in shutdown mode	V_{CC} connected to GND			-1	mA
$t_{W\_VCC(5V)}$	$\overline{CMDVCC}$ pulse width for V_{CC} = 5 V, all versions except ST8034P	See section *Section 6.10.1 on page 31*	30			ms
$t_{W\_VCC(3V)}$	$\overline{CMDVCC}$ pulse width for V_{CC} = 3 V, all versions except ST8034P	See section *Section 6.10.1 on page 31*			15	ms
Device supply voltages monitoring						
V_{TH}	Falling supply voltage threshold	V_{DD} pin	2.3	2.4	2.5	V
		V_{DDP} pin (V_{CC} = 5 V)	3.0	4.1	4.4	
		V_{DDP} pin (V_{CC} = 3 V or 1.8 V)	2.3	2.4	2.5	
		$V_{DD(INTF)}$ pin (ST8034T, ST8034AT)	1.20	1.24	1.29	
		PORADJ pin (ST8034P, ST8034C)	1.20	1.24	1.29	
V_{HYS}	Hysteresis on supply voltage threshold	V_{DD} pin	50	100	150	mV
		V_{DDP} pin (V_{CC} = 5 V)	100	200	350	
		V_{DDP} pin (V_{CC} = 3 V or 1.8 V)	50	100	150	
		$V_{DD(INTF)}$ pin (ST8034T, ST8034AT)	10	20	30	
		PORADJ pin (ST8034P, ST8034C)	10	20	30	
$I_{I(PORADJ)}$	Input current, PORADJ pin		-1		1	µA
t_W	Power-on or undervoltage reset pulse width (minimum)		5.1	8	10.2	ms

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.
2. The device can operate at V_{DD} supply voltage up to 5.5 V, however the specified parameters (mainly related to current consumption and input currents) are guaranteed in the basic V_{DD} range 2.7 to 3.6 V.
3. The device can operate at $V_{DD(INTF)}$ supply voltage up to 5.5 V, however the specified parameters (mainly related to current consumption) are guaranteed in the basic $V_{DD(INTF)}$ range 1.6 to 3.6 V.
4. These current pulses are filtered by the decoupling capacitors on the V_{CC} pin, therefore for the LDO just the mean value matters.
5. Two low ESR (< 350 mΩ) ceramic capacitors for V_{CC} decoupling recommended: 100 nF ± 20% (up to 330 nF ± 20%) close to the ST8034 and 100 nF ± 20% (up to 330 nF ± 20%) close to the card.

Table 8. Card interface

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
Data line to the card (I/O pin)[2]						
t_D	Delay time	Falling edge on pin I/O to falling edge on I/OUC or vice versa			200	ns
$t_{W(PU)}$	Pull-up pulse width		100		400	ns
f_{IO}	Input/output frequency				1	MHz
C_I	Input capacitance				10	pF
V_O	Output voltage in shutdown mode	No load	0		0.1	V
		I_O = 1 mA	0		0.3	V
I_O	Output current in shutdown mode	I/O connected to GND			-1	mA
V_{OL}	Output voltage low	I_{OL} = 1 mA	0		0.3	V
		$I_{OL} \geq$ 15 mA (current limit)	V_{CC} - 0.4		V_{CC}	
V_{OH}	Output voltage high	No load	0.9 V_{CC}		V_{CC} + 0.1	V
		I_{OH} < -40 µA (V_{CC} = 5 V or 3 V)	0.75 V_{CC}		V_{CC} + 0.1	
		I_{OH} < -20 µA (V_{CC} = 1.8 V)	0.75 V_{CC}		V_{CC} + 0.1	
		$I_{OH} \geq$ -15 mA (current limit)	0		0.4	
V_{IL}	Input voltage low		-0.3		0.8	V
V_{IH}	Input voltage high	V_{CC} = 5 V	0.6 V_{CC}		V_{CC} + 0.3	V
		V_{CC} = 3 V	0.7 V_{CC}		V_{CC} + 0.3	
V_{HYS}	Hysteresis	I/O pin		50		mV
I_{IL}	Input current low	I/O pin, V_{IL} = 0 V			750	µA
I_{IH}	Input current high	I/O pin, V_{IH} = V_{CC}			10	µA
$t_{R(I)}$	Input rise time	V_{IL} max. to V_{IH} min.			0.15	µs
$t_{R(O)}$	Output rise time	$C_L \leq$ 80 pF, 10% to 90%, 0 V to V_{CC}			0.1	µs
$t_{F(I)}$	Input fall time	V_{IL} max. to V_{IH} min.			0.15	µs
$t_{F(O)}$	Output fall time	$C_L \leq$ 80 pF, 10% to 90%, 0 V to V_{CC}			0.1	µs
R_{PU}	Pull-up resistance to V_{CC}		7	9	11	kΩ
I_{PU}	Pull-up current (one-shot circuit active)	V_{OH} = 0.9 V_{CC}	-8	-6	-4	mA
Reset output to the card (RST pin)						
V_O	Output voltage in shutdown mode	No load	0		0.1	V
		I_O = 1 mA	0		0.3	
I_O	Output current in shutdown mode	RST connected to GND			-1	mA

Table 8. Card interface (continued)

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
t_D	Delay time	Between RSTIN and RST; RST enabled			2	µs
V_{OL}	Output voltage low	I_{OL} = 200 µA, V_{CC} = 5 V	0		0.3	V
		I_{OL} = 200 µA, V_{CC} = 3 V	0		0.2	
		I_{OL} = 20 mA (current limit)	V_{CC} - 0.4		V_{CC}	
V_{OH}	Output voltage high	I_{OH} = -200 µA	0.9 V_{CC}		V_{CC}	V
		I_{OH} = -20 mA (current limit)	0		0.4	
t_R	Rise time	C_L = 100 pF			0.1	µs
t_F	Fall time	C_L = 100 pF			0.1	µs
Clock output to the card (CLK pin)						
V_O	Output voltage in shutdown mode	No load	0		0.1	V
		I_O = 1 mA	0		0.3	
I_O	Output current in shutdown mode	CLK connected to GND			-1	mA
V_{OL}	Output voltage low	I_{OL} = 200 µA	0		0.3	V
		I_{OL} = 70 mA (current limit)	V_{CC} -0.4		V_{CC}	
V_{OH}	Output voltage high	I_{OH} = -200 µA	0.9 V_{CC}		V_{CC}	V
		I_{OH} = -70 mA (current limit)	0		0.4	
t_R	Rise time[3]	C_L = 30 pF			16	ns
t_F	Fall time[3]	C_L = 30 pF			16	ns
f_{CLK}	Frequency on CLK pin	Operational	0		26	MHz
DC	Duty cycle[3]	C_L = 30 pF	45		55	%
SR	Slew rate (rise and fall, C_L = 30 pF)	V_{CC} = 5 V	0.2			V/ns
		V_{CC} = 3 V	0.12			
Card detection input ($\overline{\text{PRES}}$ pin)[4]						
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{HYS}	Hysteresis			0.14 $V_{DD(INTF)}$		V
I_{IL}	Input current low	0 < V_{IL} < $V_{DD(INTF)}$			5	µA
I_{IH}	Input current high	0 < V_{IH} < $V_{DD(INTF)}$			5	µA

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.
2. With an internal 9 kΩ pull-up resistor to V_{CC}.
3. For rise and fall times and duty cycle definitions, see *Figure 7 on page 21*.
4. $\overline{\text{PRES}}$ is active low, with an internal current source of 1.25 µA to $V_{DD(INTF)}$.

Table 9. Microcontroller interface

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
Data line to the microcontroller (I/OUC pin)[2]						
t_D	Delay time	Falling edge on pin I/O to falling edge on I/OUC or vice versa			200	ns
$t_{W(PU)}$	Pull-up pulse width		100		400	ns
f_{IO}	Input/output frequency				1	MHz
C_I	Input capacitance				10	pF
V_{OL}	Output voltage low	I_{OL} = 1 mA	0		0.3	V
V_{OH}	Output voltage high	No load	0.9 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.1	V
		$I_{OH} \leq$ 40 µA, $V_{DD(INTF)}$ > 2 V	0.75 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.1	
		$I_{OH} \leq$ 20 µA, $V_{DD(INTF)}$ < 2 V	0.75 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.1	
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{HYS}	Hysteresis	I/OUC pin		0.14 $V_{DD(INTF)}$		V
I_{IL}	Input current low	V_{IL} = 0 V			500	µA
I_{IH}	Input current high	$V_{IH} = V_{DD(INTF)}$			10	µA
R_{PU}	Pull-up resistance to $V_{DD(INTF)}$		8	10	12	kΩ
I_{PU}	Pull-up current (one-shot circuit active)	V_{OH} = 0.9 $V_{DD(INTF)}$	-1			mA
$t_{R(I)}$	Input rise time	V_{IL} max. to V_{IH} min.			0.15	µs
$t_{R(O)}$	Output rise time	$C_L \leq$ 30 pF, 10% to 90%, 0 V to $V_{DD(INTF)}$			0.1	µs
$t_{F(I)}$	Input fall time	V_{IL} max. to V_{IH} min.			0.15	µs
$t_{F(O)}$	Output fall time	$C_L \leq$ 30 pF, 10% to 90%, 0 V to $V_{DD(INTF)}$			0.1	µs
Device control inputs (CLKDIV, RSTIN, VCC_SEL, CS pins)[3]						
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{HYS}	Hysteresis			0.14 $V_{DD(INTF)}$		V

Table 9. Microcontroller interface (continued)

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
I_{IL}	Input current low				1	µA
I_{IH}	Input current high				1	µA
$V_{IL(VCC\_SEL)}$	Input voltage low	ST8034P only. The low/floating threshold is subject to minor variations.	-0.3		0.3 $V_{DD(INTF)}$	V
$V_{IH(VCC\_SEL)}$	Input voltage high	ST8034P only. The floating/high threshold is subject to minor variations.	0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ +0.3	V
$I_{IL(VCC\_SEL)}$	Input current low	ST8034P only	-30			µA
$I_{IH(VCC\_SEL)}$	Input current high	ST8034P only			30	µA
Device control input $\overline{CMDVCC}$[4]						
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{HYS}	Hysteresis			0.14 $V_{DD(INTF)}$		V
I_{IL}	Input current low	V_{IL} = 0 V			1	µA
I_{IH}	Input current high	V_{IH} = $V_{DD(INTF)}$			1	µA
$f_{\overline{CMDVCC}}$	Frequency at $\overline{CMDVCC}$ pin				100	Hz
$\overline{OFF}$ output[5]						
V_{OL}	Output voltage low	I_{OL} = 2 mA	0		0.3	V
V_{OH}	Output voltage high	I_{OH} = -15 µA	0.75 $V_{DD(INTF)}$			V
R_{PU}	Pull-up resistance to $V_{DD(INTF)}$		16	20	24	kΩ

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.
2. With an internal 10 kΩ pull-up resistor to $V_{DD(INTF)}$.
3. For clock frequency division control (CLKDIV), see *Table 13 on page 25*.
4. $\overline{CMDVCC}$ is active low.
5. $\overline{OFF}$ is an NMOS open drain, with an internal 20 kΩ pull-up resistor to $V_{DD(INTF)}$.

Table 10. Clock circuits

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
Input for external clock (CLKIN pin - ST8034P, ST8034C)						
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
I_{IL}	Input current low	V_{IL} = 0 V			1	µA
I_{IH}	Input current high	V_{IH} = $V_{DD(INTF)}$			1	µA
$t_{R(I)}$	Input rise time	V_{IL} max. to V_{IH} min.			10	ns
$t_{F(I)}$	Input fall time	V_{IL} max. to V_{IH} min.			10	ns
f_{CLKIN}	External clock frequency	External clock on CLKIN pin	0.032		26	MHz
Internal oscillator						
$f_{OSC(INT)LOW}$	Internal oscillator frequency	Shutdown mode	100	150	200	kHz
$f_{OSC(INT)}$		Active state	2	2.7	3.2	MHz
Crystal oscillator (XTAL1 and XTAL2 pins)						
C_{EXT}	External capacitances	XTAL1 and XTAL2 to GND (according to the crystal or resonator specification)			15	pF
f_{XTAL}	External crystal frequency	Card clock reference, crystal oscillator	2		26	MHz
f_{EXT}	External clock frequency	External clock on XTAL1	0.032		26	MHz
$t_{R(fEXT)}$	External clock frequency rise time	External clock on XTAL1			10	ns
$t_{F(fEXT)}$	External clock frequency fall time	External clock on XTAL1			10	ns
V_{IL}	Input voltage low	Crystal oscillator	-0.3		0.3 V_{DD}	V
		External clock on XTAL1	-0.3		0.3 $V_{DD(INTF)}$	
V_{IH}	Input voltage high	Crystal oscillator	0.7 V_{DD}		V_{DD} + 0.3	V
		External clock on XTAL1	0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.

Table 11. Protection characteristics

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
I_{OLIM}	Output current limit(2)	I/O pin	-15		15	mA
		CLK pin	-70		70	
		RST pin	-20		20	
$I_{SD(VCC)}$	Limit and shutdown card supply current	V_{CC} pin	90	120	150	mA
T_{SD}	Shutdown junction temperature			150		°C

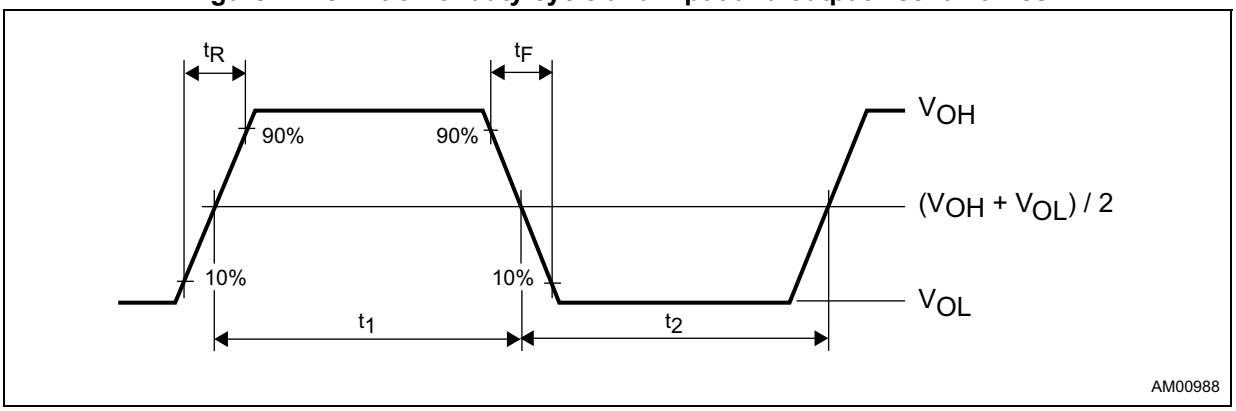
1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.
2. All card contacts are protected against short-circuit to any other card contact.

Table 12. Timing characteristics

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
t_{ACT}	Activation time	See *Figure 12 on page 27*	2090		4160	µs
t_{DEACT}	Deactivation time	See *Figure 13 on page 28*	35	90	250	µs
$t_{D(START)}$, $t_{D(END)}$	Delay time, CLK sent to card using an external clock	$t_{D(START)} = t_3$, see *Figure 12 on page 27*	2090		4112	µs
		$t_{D(END)} = t_5$, see *Figure 12 on page 27*	2120		4160	
t_{DEB}	Debounce time	$\overline{PRES}$ pin	3.2	4.5	6.4	ms

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.

Figure 7. Definition of duty cycle and input and output rise/fall times



Duty cycle (DC) = $t_1 / (t_1 + t_2)$.

6 Functional description

Throughout this document it is assumed that the reader is familiar with ISO7816 terminology.

6.1 Power supplies

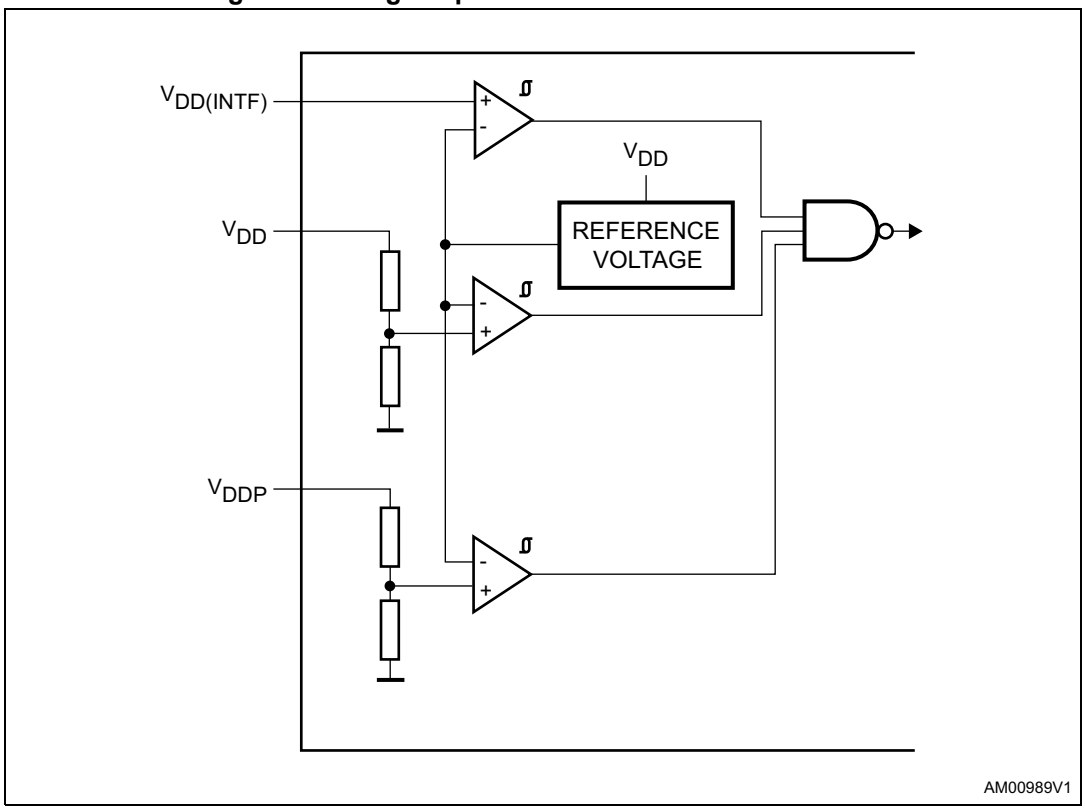
All interface signals to the host microcontroller are referenced to $V_{DD(INTF)}$. All card contacts remain inactive during power-up or power-down. After powering-up the device, $\overline{OFF}$ output remains low until CMDVCC input is set high and PRES input is low. During power-down, $\overline{OFF}$ output goes low when V_{DDP} falls below the V_{DDP} falling threshold voltage. The internal oscillator clock frequency $f_{OSC(INT)}$ is used only during the activation sequence. When the card is not activated (CMDVCC input is high), the internal oscillator is in low frequency mode to reduce power consumption.

Power-on sequence: supply voltages may be applied to the ST8034 in any sequence.

6.2 Voltage supervisor

6.2.1 Voltage supervisor ST8034T and ST8034AT

Figure 8. Voltage supervisor - ST8034T and ST8034AT



The voltage supervisor monitors the voltage of the V_{DD}, V_{DDP} and $V_{DD(INTF)}$ supplies and provides both power-on reset (POR) and supply dropout detection during a card session. The supervisor threshold voltages for V_{DD}, V_{DDP} and $V_{DD(INTF)}$) are set internally. As long as V_{DD}, V_{DDP} or $V_{DD(INTF)}$ is less than the corresponding V_{TH} + V_{HYS}, the ST8034 device remains inactive irrespective of the command line levels. After V_{DD}, V_{DDP}, and $V_{DD(INTF)}$ have reached a level higher than the corresponding V_{TH} + V_{HYS}, the device still remains inactive for the duration of t_W, a defined reset pulse of approximately 8 ms (t_W = 1024 x 1/$f_{OSC(INT)LOW}$) when the output of the supervisor keeps the control logic in reset state. This is used to maintain the device in shutdown mode during the supply voltage power-on, see *Figure 10*. A deactivation sequence is performed when either V_{DD}, V_{DDP} or $V_{DD(INTF)}$ falls below the corresponding V_{TH}.

6.2.2 Voltage supervisor with PORADJ function (ST8034P and ST8034C)

In the case of devices with the PORADJ pin (ST8034P, ST8034C), additional flexibility of the voltage monitoring is available: the PORADJ pin provides an independent voltage monitoring input that can be used for $V_{DD(INTF)}$ monitoring (as shown in *Figure 9*) or generally for the monitoring of any external voltage to which the resistor divider is connected, with adjustable threshold.

Undervoltage (UVLO) threshold adjustment on the PORADJ input with the resistor divider:

$V_{DD(INTF)}$ UVLO threshold (falling) = (R1+R2)/R2 x $V_{TH(PORADJ)}$

$V_{DD(INTF)}$ UVLO threshold (rising) = (R1+R2)/R2 x ($V_{TH(PORADJ)}$ + $V_{HYST(PORADJ)}$)

If the external resistor divider is not used, connect the PORADJ pin to $V_{DD(INTF)}$, then $V_{DD(INTF)}$ UVLO threshold = $V_{TH(PORADJ)}$.

Figure 9. Voltage supervisor with adjustable $V_{DD(INTF)}$ threshold (PORADJ function) - ST8034P and ST8034C

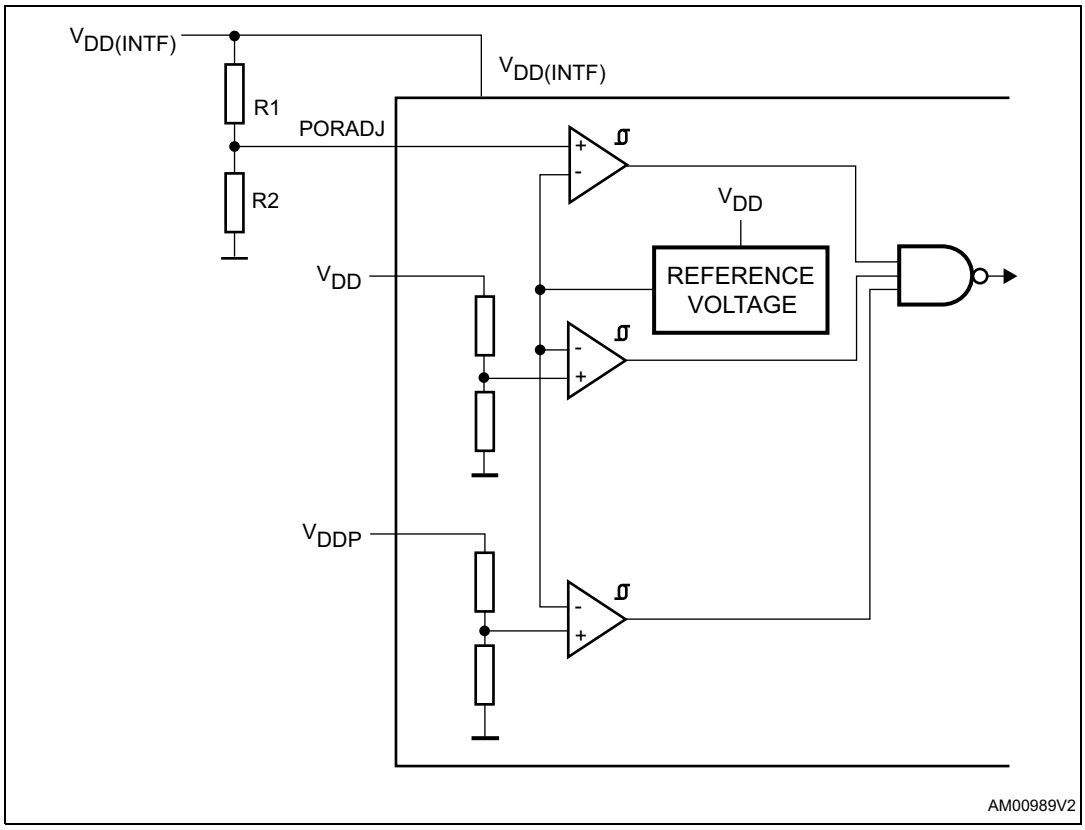
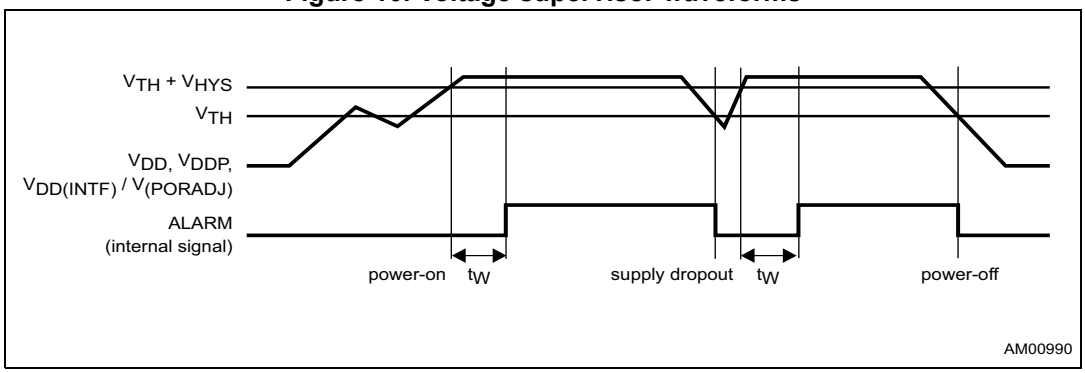


Figure 10. Voltage supervisor waveforms

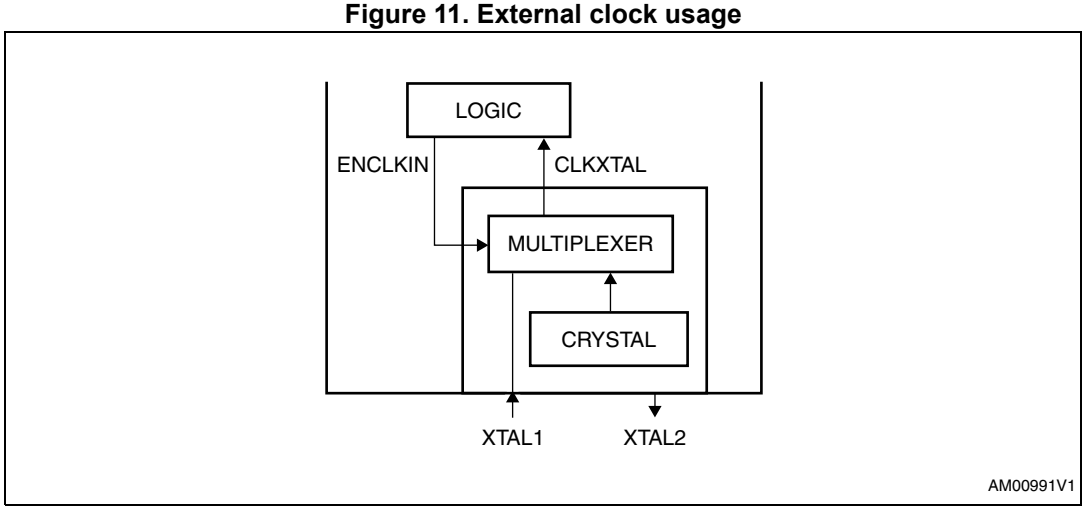


6.3 Clock circuits

6.3.1 ST8034T and ST8034AT clock possibilities

The clock signal for the card (CLK output) is either provided by an external clock signal connected to the XTAL1 pin or generated by a crystal connected between the XTAL1 and XTAL2 pins. The ST8034 device automatically detects if an external clock is connected to the XTAL1, which eliminates the need for a separate clock source selection pin. Automatic clock source detection is performed on each activation command (falling edge of $\overline{\text{CMDVCC}}$). The presence of an external clock on the XTAL1 pin is checked during a time window defined by the internal oscillator. If the external clock is detected, the crystal oscillator is stopped. If the clock is not detected, the crystal oscillator is started. When the external clock is used, the clock signal must be present on the XTAL1 pin before the $\overline{\text{CMDVCC}}$ falling edge. If the external clock is used, connect it to XTAL1 input and leave the XTAL2 pin floating. The XTAL1 pin cannot be left floating, either a crystal or an external clock source needs to be connected.

Figure 11. External clock usage



The clock frequency is selected using the CLKDIV pin and is either $f_{XTAL}/2$ or $f_{XTAL}/4$ on the ST8034T device or f_{XTAL} or $f_{XTAL}/2$ on the ST8034AT, as shown in *Table 13*. The frequency change is synchronous, meaning that after transition on the CLKDIV input, the present clock period is completed and after that the new whole clock period starts, therefore no clock period is shortened during the frequency switchover.

If an external crystal is used, the duty cycle on the CLK pin should be between 45% and 55%. If an external clock is connected to the XTAL1 pin, its duty cycle must be between 48% and 52% so that the CLK output duty cycle is between 45% and 55%.

Table 13. ST8034T and ST8034AT clock frequency selection

CLKDIV pin level	CLK frequency	
	ST8034T	ST8034AT
High	$f_{XTAL}/2$	$f_{XTAL}/2$
Low	$f_{XTAL}/4$	f_{XTAL}

6.3.2 ST8034P and ST8034C clock

In the case of ST8034P and ST8034C, only one external clock input (CLKIN) is implemented, referred to $V_{DD(INTF)}$, with identical functionality such as use of the XTAL1 pin in the case of ST8034T or ST8034AT.

6.4 Input and output circuits

When the I/O and I/OUC pins are pulled high by a 9 kΩ resistor between I/O and V_{CC} and/or 10 kΩ resistor between I/OUC and $V_{DD(INTF)}$, both lines enter the idle state. The I/O pin is referenced to V_{CC} and the I/OUC pin to $V_{DD(INTF)}$, which allows operation at V_{CC} level different from $V_{DD(INTF)}$ level.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables falling edge detection on the other side, making it the slave. After a time delay t_D, the logic 0 present on the master side is sent to the slave side. When the master side returns logic 1, the slave side sends logic 1 during time delay ($t_{W(PU)}$). After this sequence, both master and slave sides return to their idle states.

The active pull-up feature (one-shot circuit) ensures fast low to high transitions, making the ST8034 outputs capable of delivering more than 1 mA, up to an output voltage of 0.9 V_{CC}, at a load of 80 pF. At the end of the active pull-up pulse, the output voltage is dependent on the internal pull-up resistor value and load current. The current sent to and received from the card's I/O lines is limited to 15 mA at a maximum frequency of 1 MHz.

6.5 Shutdown mode

After a power-on reset, if $\overline{\text{CMDVCC}}$ is high, the ST8034 device enters shutdown mode, ensuring only the minimum number of circuits are active while the ST8034 device waits for the microcontroller to start a session.

- All card contacts are inactive. The impedance between the contacts and GND is approximately 200 Ω
- I/OUC pin is in high impedance with the 10 kΩ pull-up resistor connected to $V_{DD(INTF)}$
- The voltage generators are stopped
- The voltage supervisor is active
- The internal oscillator runs at its low frequency ($f_{OSC(INT)LOW}$).

6.6 Activation sequence

The following device activation sequence is applied when using an external clock, see also *Figure 12*.

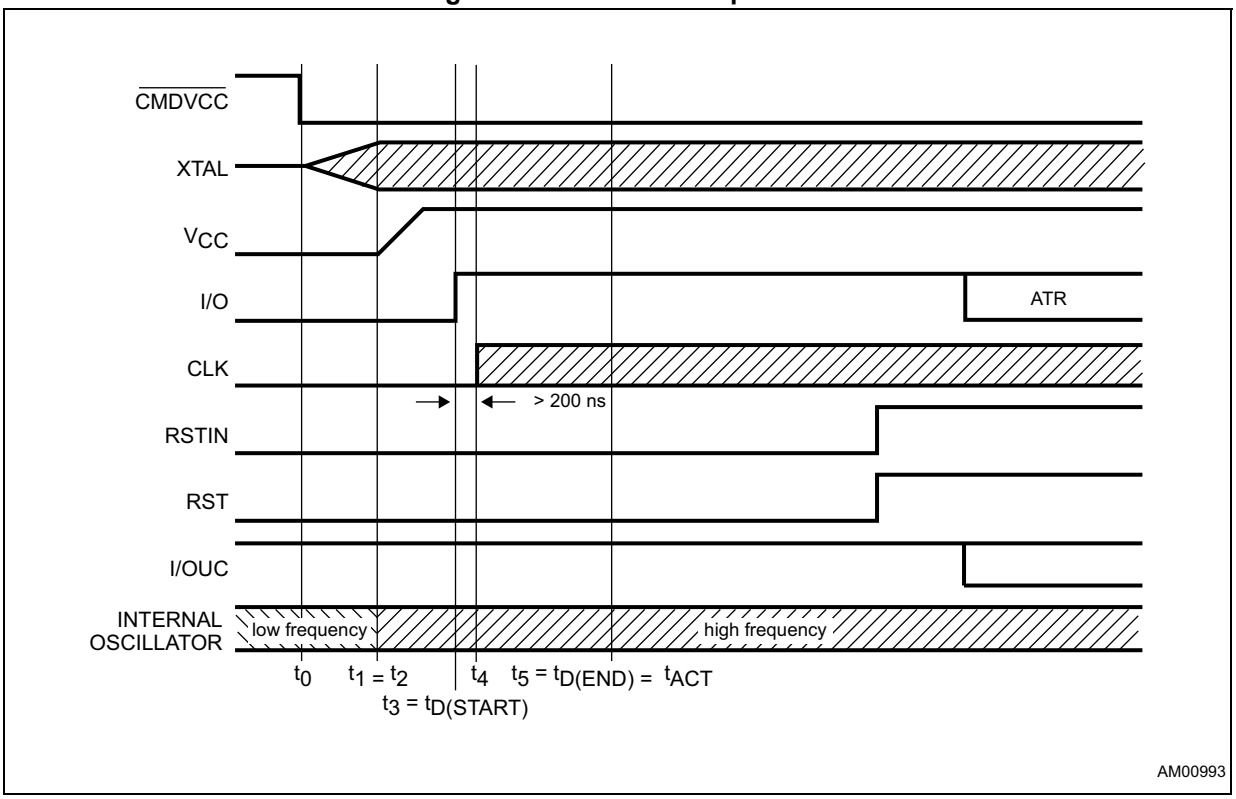
1. $\overline{\text{CMDVCC}}$ is pulled low (t_0).
2. The internal oscillator is triggered (t_0).
3. The internal oscillator changes to high frequency (t_1).
4. V_{CC} rises from 0 V to 3 V or to 5 V (or to 1.8 V in the case of ST8034P) on a controlled slope (t_2).
5. I/O is driven high (t_3).
6. The clock on the CLK output is applied to the C3 contact (t_4).
7. RST is enabled (t_5).

Time delays

- $t_1 = t_0 + 384 \times 1/f_{OSC(INT)LOW}$
- $t_2 = t_1$
- t_3 ($t_{D(START)}$) = t_1 + 17T/2
- t_4 = driven by host microcontroller, $t_5 > t_4 > t_3$
- t_5 ($t_{D(END)}$) = t_1 + 23T/2.

$T = 64 \times 1/f_{OSC(INT)}$

Figure 12. Activation sequence



6.7 Deactivation sequence

When a session ends, the microcontroller sets $\overline{\text{CMDVCC}}$ high. The ST8034 device then executes an automatic deactivation sequence by counting the sequencer back to the inactive state (see *Figure 13*):

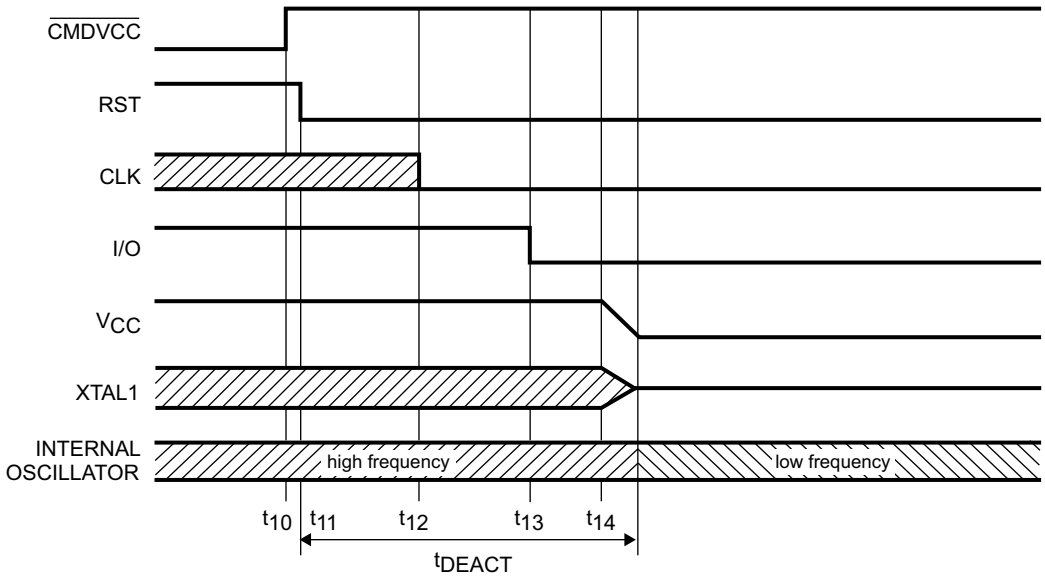
1. RST goes low (t_{11}).
2. The clock is stopped, CLK is low (t_{12}).
3. I/O is pulled low (t_{13}).
4. V_{CC} falls to 0 V (t_{14}). The deactivation sequence is completed when V_{CC} reaches its inactive state.
5. V_{CC} < 0.4 V (t_{DEACT}).
6. All card contacts become low impedance to GND. The I/OUC pin remains pulled up to $V_{DD(INTF)}$ by the internal 10 kΩ pull-up resistor.
7. The internal oscillator returns to its low frequency mode.

Time delays

- $t_{11} = t_{10} + 3T / 64$
- $t_{12} = t_{11} + T / 2$
- $t_{13} = t_{11} + T$
- $t_{14} = t_{11} + 3T / 2$
- $t_{DEACT} = t_{11} + 3T / 2 + V_{CC}$ fall time.

$T = 64 \times 1/f_{OSC(INT)}$

Figure 13. Deactivation sequence



6.8 V_{CC} generator

The LDO on the V_{CC} output is capable of supplying up to 65 mA continuously at any selected V_{CC} value (5 V or 3 V, or even 1.8 V in the case of ST8034P). This output is overcurrent protected by a current limiter with a limit threshold value of 120 mA typ., with a glitch immunity allowing overcurrent pulses up to 200 mA with duration up to several microseconds not causing a deactivation (the average current value must stay below the specified current limit, see *Table 7 on page 14* and *Table 11 on page 21*).

A 100 nF capacitor (min.) with ESR < 350 mΩ should be tied to GND near the V_{CC} pin and another low ESR 100 nF capacitor (min.) should be tied to GND also on the card side, near the card reader contact C1.

6.9 Fault detection

The fault conditions monitored by the device are:

- Short-circuit or overcurrent on the V_{CC} pin
- Card removal during transaction
- V_{DD} falling
- V_{DDP} falling
- $V_{DD(INTF)}$ falling
- Overheating.

There are two different fault detection situations:

- Outside card session ($\overline{CMDVCC}$ pin is high): the $\overline{OFF}$ pin is low if the card is not in the reader and high if the card is in the reader. Any voltage drop on V_{DD}, V_{DDP} or $V_{DD(INTF)}$ is detected by the voltage supervisor. This generates an internal power-on reset pulse but does not act upon the $\overline{OFF}$ pin signal. The card is not powered-up and short-circuits or overheating are not detected.
- In card session ($\overline{CMDVCC}$ pin is low): when the $\overline{OFF}$ pin goes low, the fault detection circuit triggers the automatic emergency deactivation sequence (see *Figure 14*).

On card insertion or removal, bouncing can occur on the card presence switch (i.e. on the $\overline{PRES}$ signal). Therefore a debouncing feature is integrated in the ST8034 (4.5 ms typically, t_{DEB} = 640 × 1/$f_{OSC(INT)LOW}$). See *Figure 15*.

On card insertion, the $\overline{OFF}$ pin goes high after the debounce time has elapsed. When the card is extracted, the automatic card deactivation sequence is performed on the first high to low transition on the $\overline{PRES}$ pin. After this, the $\overline{OFF}$ pin goes low.

Figure 14. Deactivation sequence after card removal

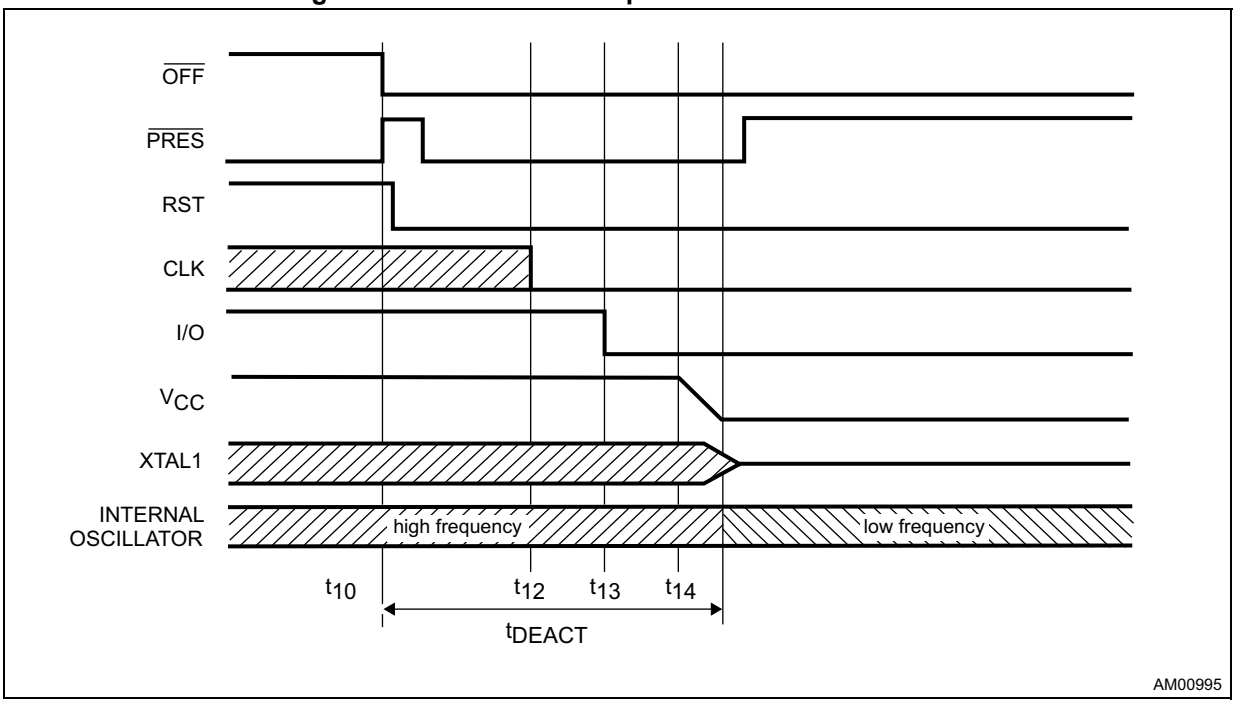
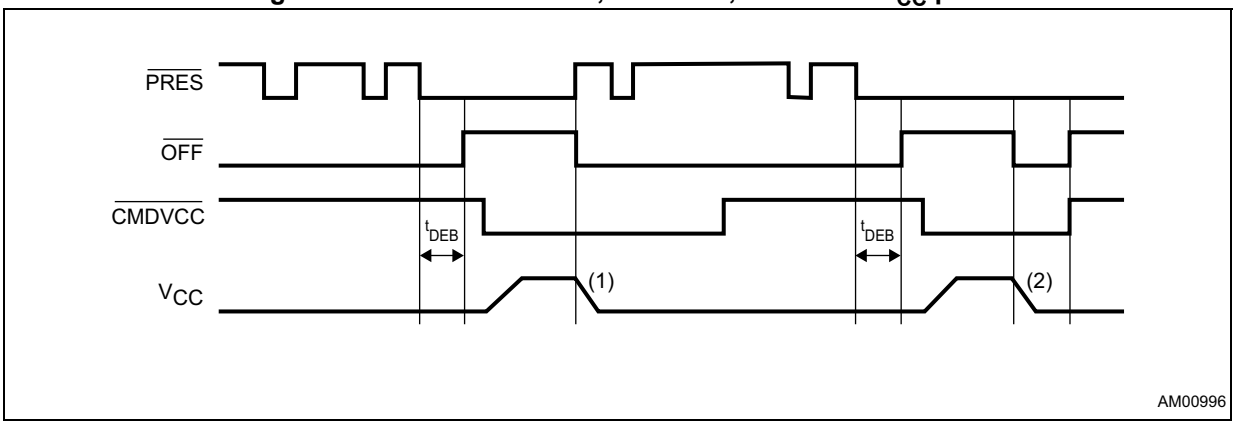


Figure 15. Debounce at $\overline{OFF}$, $\overline{CMDVCC}$, $\overline{PRES}$ and V_{CC} pins



1. Deactivation caused by card withdrawal.
2. Deactivation caused by short-circuit on card side.

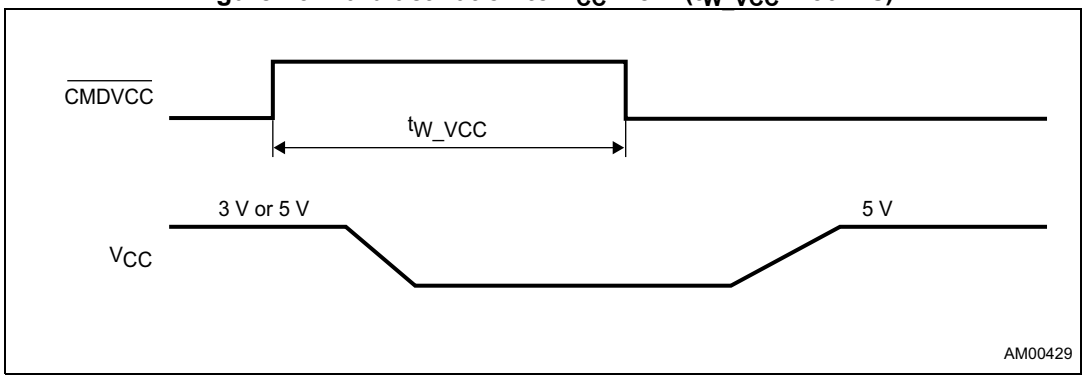
6.10 Card supply voltage (V_{CC}) selection

6.10.1 Automatic determining of card supply voltage (V_{CC}) - all versions except ST8034P

The supply voltage (V_{CC}) that the card requires is determined automatically by monitoring the duration of the high state on the $\overline{CMDVCC}$ pin before the activation command $\overline{CMDVCC}$ falling edge occurs. If the $\overline{CMDVCC}$ pin stays high for more than 30 ms (t_{W_VCC}), the activation is done with V_{CC} = 5 V. If the $\overline{CMDVCC}$ pin stays high for less than 15 ms, the activation is done with V_{CC} = 3 V.

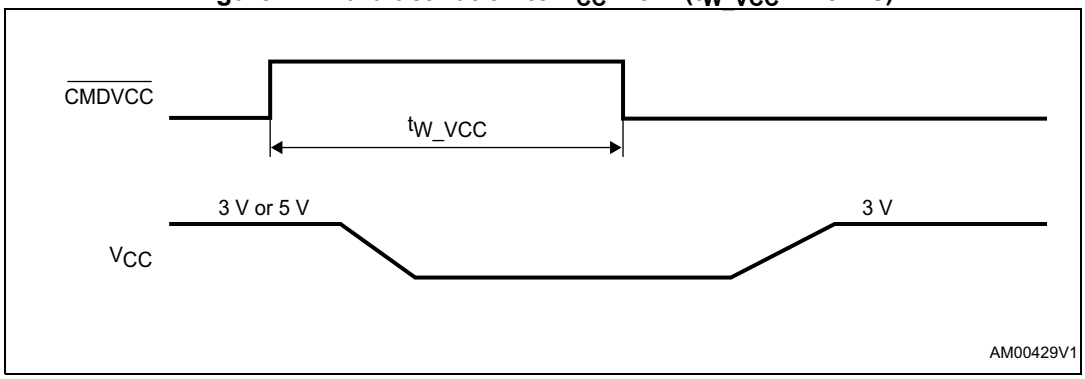
To activate the card at V_{CC} = 5 V, the $\overline{CMDVCC}$ pin must stay high for t_{W_VCC} > 30 ms before going low:

Figure 16. Card activation to V_{CC} = 5 V (t_{W_VCC} > 30 ms)



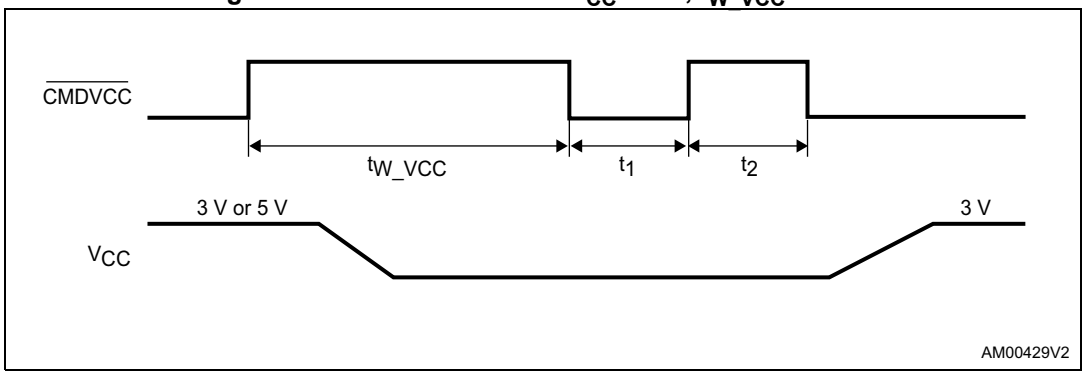
To activate the card at V_{CC} = 3 V, the $\overline{CMDVCC}$ pin must stay high for t_{W_VCC} < 15 ms before going low:

Figure 17. Card activation to V_{CC} = 3 V (t_{W_VCC} < 15 ms)



If the $\overline{\text{CMDVCC}}$ pin is high for more than 15 ms but less than 30 ms (15 ms < t_{W_VCC} < 30 ms), the $\overline{\text{CMDVCC}}$ pin must be set low for t_1 (200 µs < t_1 < 700 µs) and then high for t_2 (200 µs < t_2 < 15 ms) before going low:

Figure 18. Card activation to V_{CC} = 3 V, t_{W_VCC} >15 ms



If the $\overline{\text{CMDVCC}}$ pin is high for more than 30 ms (card inactive), and if the card needs to be activated at 3 V, the sequence shown in *Figure 18* applies: the $\overline{\text{CMDVCC}}$ pin must be set low for t_1 (200 µs < t_1 < 700 µs) and then high for t_2 (200 µs < t_2 < 15 ms) before going low.

6.10.2 Card supply (V_{CC}) selection by tristate VCC_SEL pin (ST8034P only)

For the ST8034P device, a 1.8 V card supply feature was added and all the 5 V, 3 V or 1.8 V card supply (V_{CC}) levels are pin-selectable by the single VCC_SEL input pin which works in a tristate mode, see *Table 14*. To define a logic level in the case of the “left-floating” state, an internal resistor divider (285 + 285 kΩ) between $V_{DD(INTF)}$ and GND is implemented on this pin. The V_{CC} voltage value should not be increased in active mode, as this could cause an overcurrent condition and deactivation due to an attempt to step change the voltage on the C_{VCC} capacitor.

Table 14. ST8034P V_{CC} selection

VCC_SEL pin level	VCC output (card supply) voltage [V]
High	5
Low	3
Floating	1.8

6.11 Chip select (ST8034C only)

The chip select (CS) input is active high, meaning normal operation when the CS input is in logic high state. When the CS pin goes low, the status of the ST8034C device is frozen (i.e. the status of control inputs RSTIN and $\overline{\text{CMDVCC}}$ is latched) and the I/OUC pin on the microcontroller interface goes into a high impedance mode (with pull-up resistor to $V_{DD(INTF)}$), not transferring any data to or from the card. The $\overline{\text{OFF}}$ output pin also goes into a high impedance mode. This allows the microcontroller interface pins to be shared among multiple smartcard interfaces connected in parallel. The status and all the ST8034C device functions (including the card) are maintained for immediate use when the CS goes high again. For this reason CLKIN clock input is not affected by the chip select, the clock is provided to the ST8034C device and to the card even when the CS is low.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 19. SO16 - 3.9 x 9.9 mm body package outline

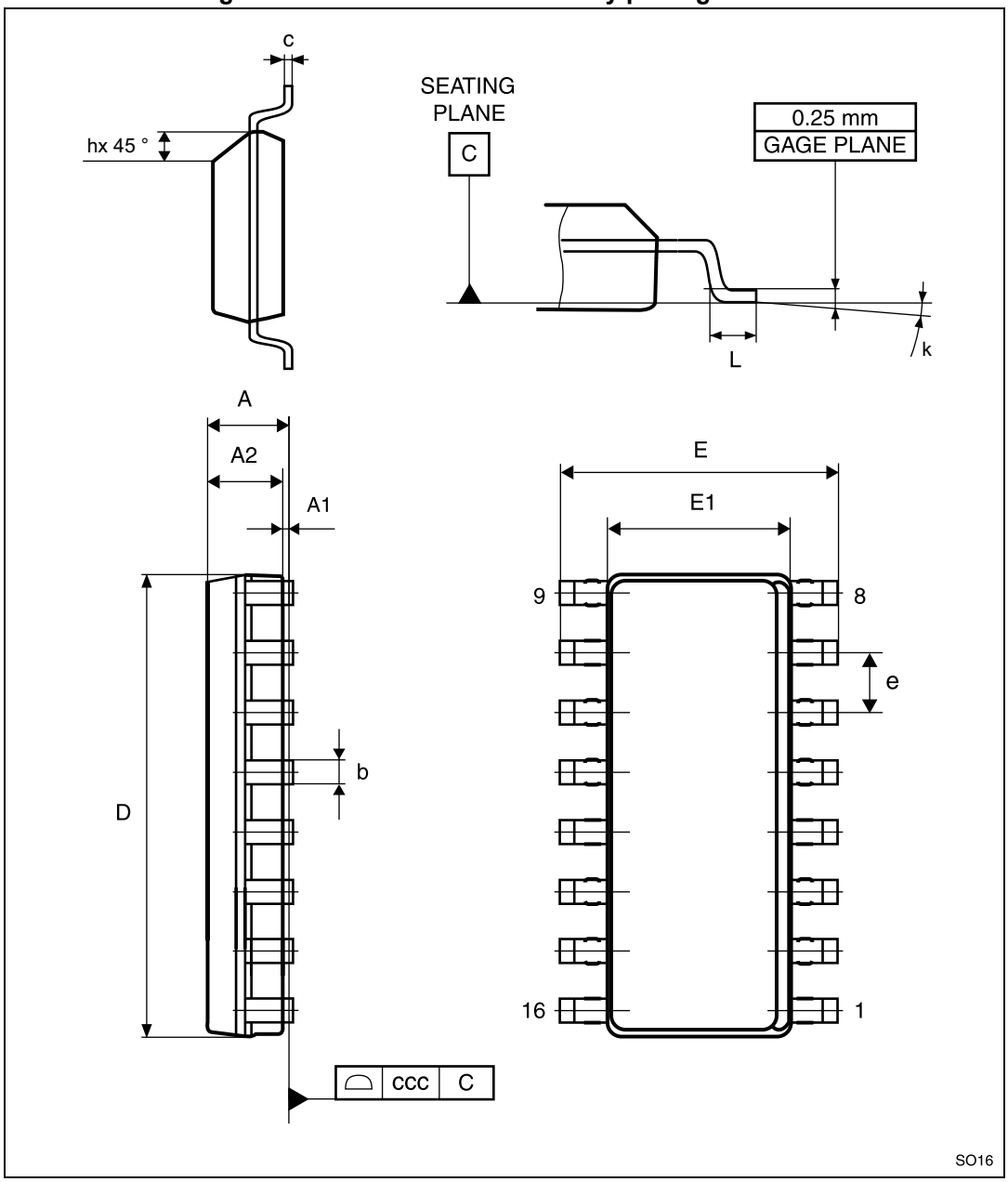


Table 15. SO16 - 3.9 x 9.9 mm body package mechanical data

Symbol	Dimensions (mm)			Notes
	Min.	Typ.	Max.	
A			1.75	
A1	0.10		0.25	
A2	1.25			
b	0.31		0.51	
c	0.17		0.25	
D	9.80	9.90	10.00	(1)
E	5.80	6.00	6.20	
E1	3.80	3.90	4.00	(2)
e		1.27		
h	0.25		0.50	
L	0.40		1.27	
k	0		8	(3)
ccc			0.10	

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs should not exceed 0.15 mm in total (both sides).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions should not exceed 0.25 mm (per side).
3. Degrees.

Figure 20. Recommended footprint SO16 - 3.9 x 9.9 mm body

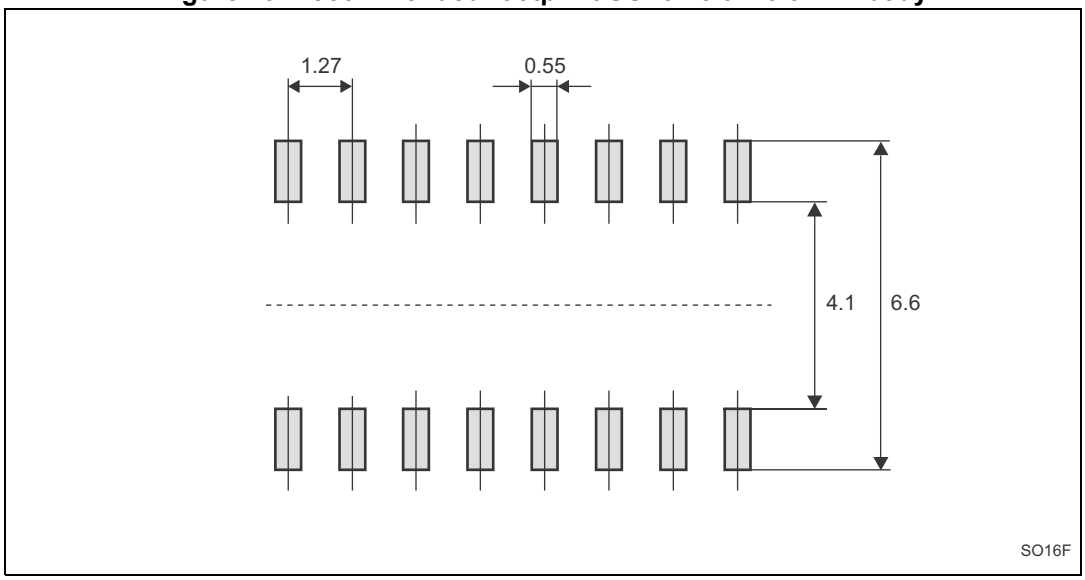


Figure 21. QFN16 - 3 x 3 x 0.8 mm, 0.5 mm pitch package outline

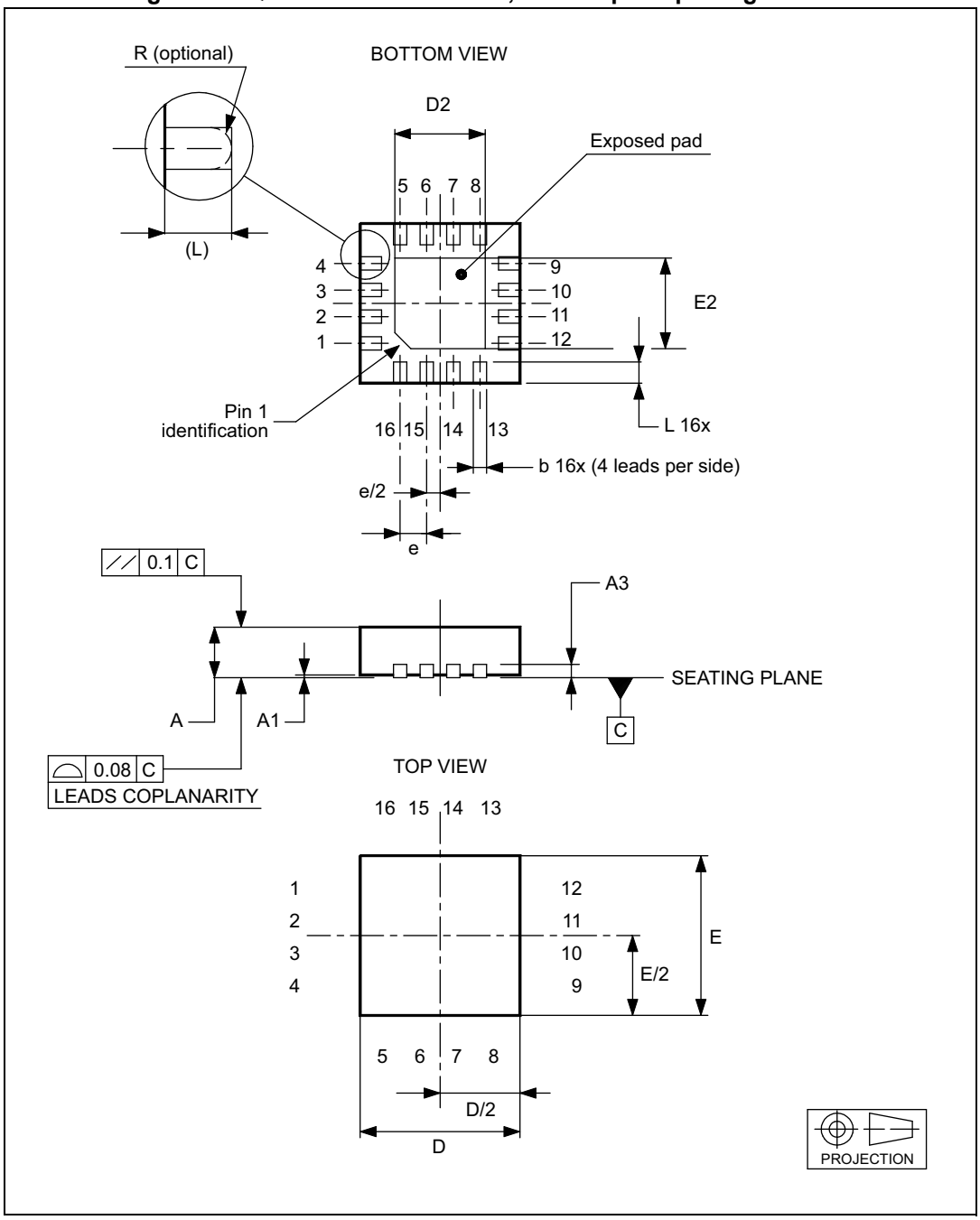
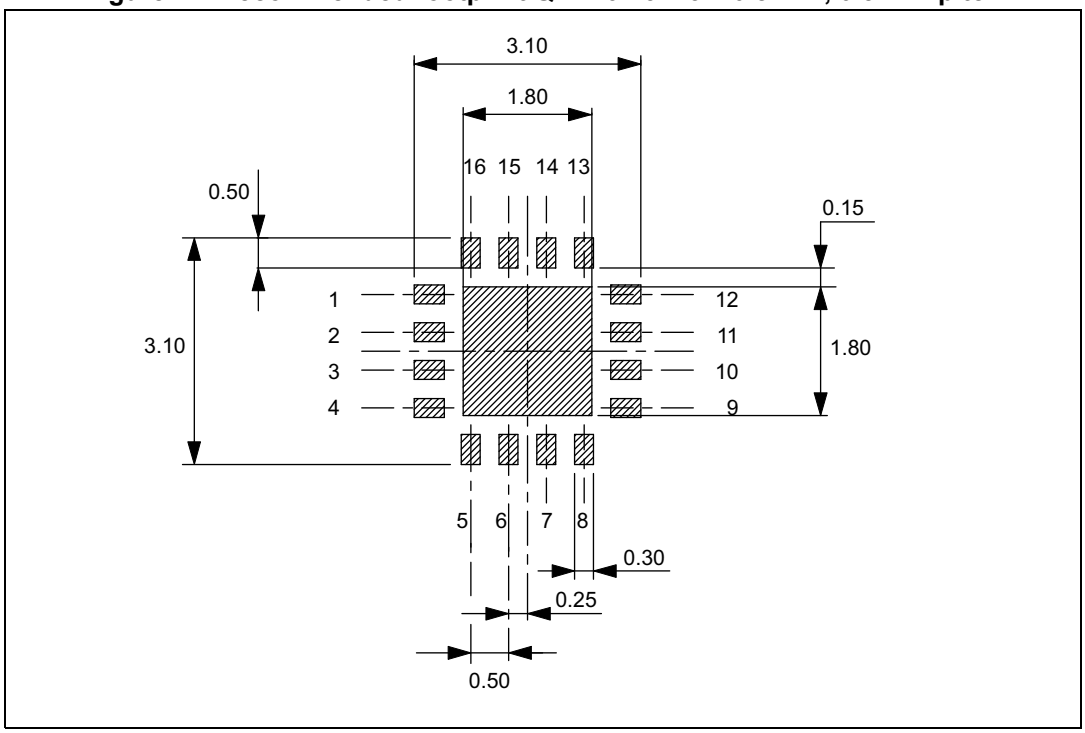


Table 16. QFN16 - 3 x 3 x 0.8 mm, 0.5 mm pitch package mechanical data(1), (2), (3)

Symbol	Dimensions (mm)			Note
	Nom.	Min.	Max.	
A	0.75	0.70	0.80	
A1	0.02	0	0.05	
A3	0.20			
b	0.25	0.18	0.30	
D	3	2.90	3.10	
D2	1.70	1.50	1.80	
E	3	2.90	3.10	
E2	1.70	1.50	1.80	
e	0.50			
L	0.40	0.30	0.50	(4)

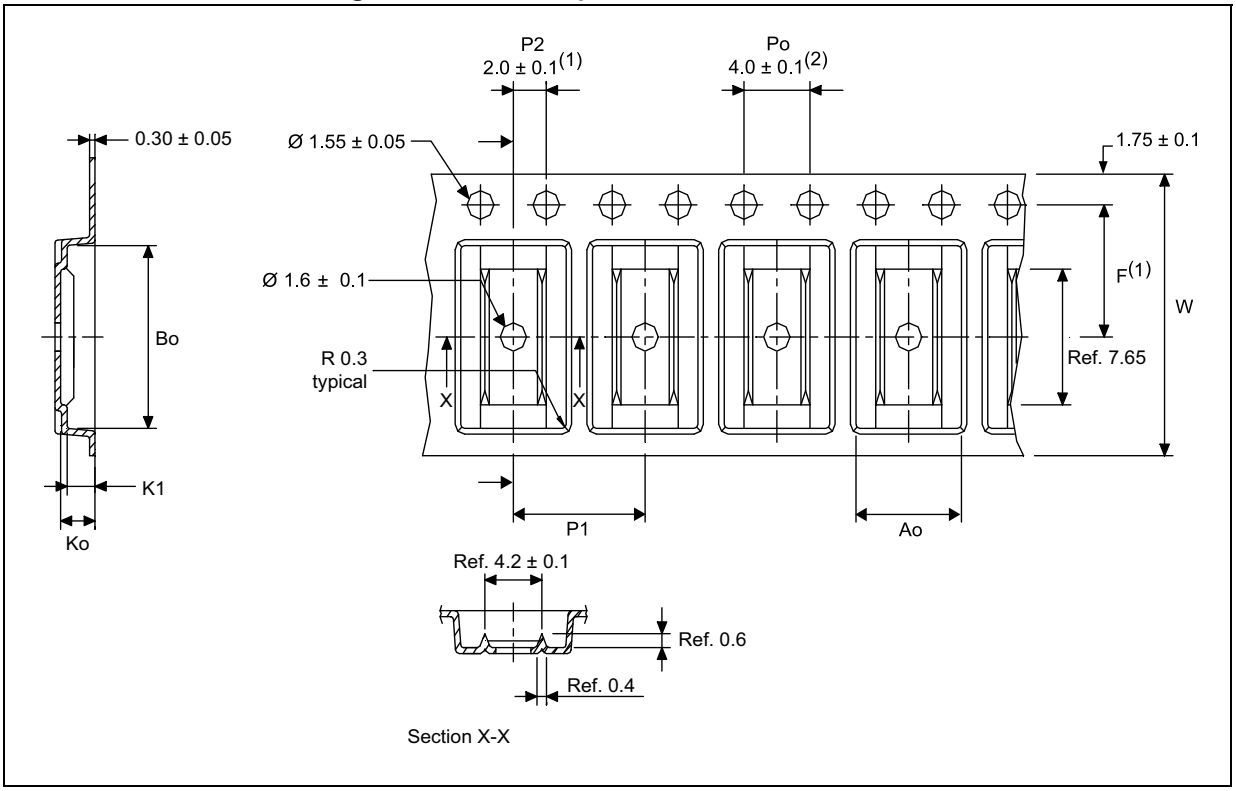
1. The lead size is comprehensive of the thickness of the lead finishing material.
2. Dimensions do not include mold protrusion, not to exceed 0.15 mm.
3. Package outline exclusive of metal burr dimensions.
4. The value of “L” a JEDEC norm is min. 0.35 - max. 0.45.

Figure 22. Recommended footprint QFN16 - 3 x 3 x 0.8 mm, 0.5 mm pitch



8 Tape and reel information

Figure 23. Carrier tape for SO16 - 3.9 x 9.9 mm

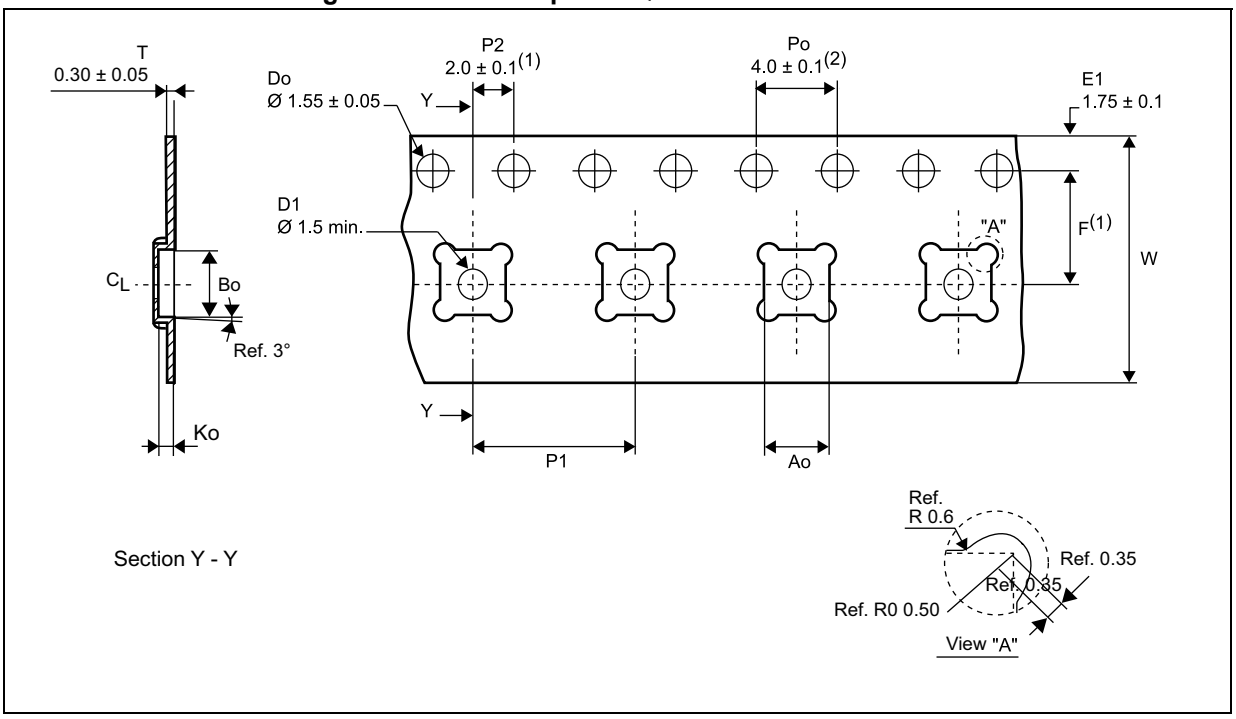


1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ± 0.20.
3. Other material available.
4. All dimensions are in millimeters unless otherwise stated.

Table 17. Dimensions of carrier tape for SO16 - 3.9 x 9.9 mm

Ao	Bo	Ko	K1	F	P1	W
6.55 ± 0.1	10.38 ± 0.1	2.10 ± 0.1	1.80 ± 0.1	7.50 ± 0.1	8.00 ± 0.1	16.00 ± 0.3

Figure 24. Carrier tape for QFN16 - 3 x 3 x 0.55 mm



1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ± 0.20.
3. Other material available.
4. Typical SR of form tape from 10^5 to 10^{10} Ω/sq.
5. All dimensions are in millimeters unless otherwise stated.

Table 18. Dimensions of carrier tape for QFN16 - 3 x 3 x 0.55 mm

Ao	Bo	Ko	F	P1	W
3.30 ± 0.1	3.30 ± 0.1	0.80 ± 0.1	5.50 ± 0.1	8.00 ± 0.1	12.00 ± 0.3

Table 19. Tape and reel specification QFN16

Quantity per reel	Carrier tape		Cover tape		Lockreel 7 / 13"	
	Part no. (vendor)	Description	Part no. (vendor)	Description	Part no. (vendor)	Description
3000	434146 (Cpak)	Carrier tape 12 mm width, 8 mm pitch	437150 (Cpak)	Cover tape 9.2 mm width	434543 (peak)	13" lockreel

9 Revision history

Table 20. Document revision history

Date	Revision	Changes
06-May-2013	1	Initial release.
17-Jul-2013	2	– Removed footnote reference from ST8034P in *Table 1: Device summary*. – Updated $I_{DD(INTF)}$ maximum value in *Table 7: Supply voltages* – Modified *Figure 4: Pin connections ST8034T and ST8034AT, top view*. – Added sentence to the end of *Section 6.10.2: Card supply (V_{CC}) selection by tristate VCC_SEL pin (ST8034P only)*.
26-Aug-2013	3	– Removed footnote reference from ST8034T in *Table 1: Device summary*. – Minor corrections throughout document.
31-Oct-2013	4	– Removed footnote reference from ST8034CQR in *Table 1: Device summary on page 6*. – Minor modifications throughout document.

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